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PCN Date: 22Jun11			Effective Date: 28Dec11		
Title: C8051F52x/F53x End of Life and Last Time Buy					
Originator: Ike Saeed Phone: 502-464-9		203	Dept: EMS Marketing		
Customer Contact: Kathy Haggar	Phone: 512-532-5261		Dept: Sales		
PCN Type:					
Assembly Discont	inuance 🗌 Pa	ackage	e 🗌 Test		
Datasheet Datasheet	ition 🗌 Pr	oduct	Revision		
Packing Labelin	g 🗌 Lo	ocatior	n 🗌 Other		
Last Order Date: 28Dec11					
PCN Details					
Description of Change:					
Silicon Laboratories is announcing the discontinuance of following products. These products are End of Life and subject to Last Time Buy restrictions.					
C8051F520-IM C80	051F534-IM				
C8051F521-IM C80	3051F521-IM C8051F537-IT				
C8051F527-IM					
C8051F530-IM					
C8051F530-IT					
C8051F531-IM					
Last-time buy orders for the above part numbers must be placed by 28Dec2011. Shipment of orders from Silicon Labs will be completed by 22Jun2012. All orders are non-cancellable and non-returnable.					
Reason for Change:					
Replaced with subsequent revisions.					
Impact on Form, Fit, Function, Quality, Reliability:					
No change to Form, Fit, Quality or Reliability. Silicon Laboratories recommends C8051F52xA/C8051F53xA as replacement parts. The C8051F52xA/F53xA devices are fully code compatible but have minor differences in behavior and pin-out. The location of the pins used by the serial UART interface is different between C8051F52x/F53x and C8051F52xA/F53xA devices. The behavioral differences between discontinued C8051F52x/F53x devices and replacement C8051F52xA/F53xA devices are described in Appendix A and are also included in section 20 of C8051F52x/F52xA/F53x/F53xA datasheet available from www.silabs.com.					

W7206F1 Process Change Notice Form rev AA

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Product Identification:		
Discontinued Products	Recommended Replacement	
C8051F520-IM	C8051F520A-IM	
C8051F521-IM	C8051F521A-IM	
C8051F527-IM	C8051F527A-IM	
C8051F530-IM	C8051F530A-IM	
C8051F530-IT	C8051F530A-IT	
C8051F531-IM	C8051F531A-IM	
C8051F534-IM	C8051F534A-IM	
C8051F537-IT	C8051F537A-IT	

Last Date of Unchanged Product:

Last-time buy orders for the C8051F52x/F53x must be placed by 28Dec2011. Shipment of orders from Silicon Labs will be completed by 22Jun2012. All orders are non-cancellable and non-returnable.

Qualification Samples:

All replacement products are at full production status. Samples are available upon request. Please contact your local Silicon Laboratories sales representative to order samples. A list of Silicon Laboratories sales representatives may be found at <u>www.silabs.com</u>

Customer Early Acceptance Sign Off:

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance Date:

Name:

Company:

Email your early Acceptance approval to: <u>katherine.haggar@silabs.com</u>

Qualification Data: N/A



APPENDIX A - C8051F52x/F53x and C8051F52xA/F53xA Behavioral Differences

Reset Pin Behavior: The reset behavior of C8051F52x/F53x differs from C8051F52xA/F53xA devices. The differences affect the state of the RST pin during a VDD Monitor reset. On C8051F52x/F53x devices, a VDD Monitor reset does not affect the state of the RST pin. On C8051F52xA/F53xA devices, a VDD Monitor reset will pull the RST pin low for the duration of the brownout condition.

Reset Time Delay: The reset time delay on C8051F52x/F53x devices differs from C8051F52xA/F53xA devices. On C8051F52x/F53x devices, the reset time delay will be as long as 80 ms following a power-on reset, meaning it can take up to 80 ms to begin code execution. Subsequent resets will not cause the long delay. On C8051F52xA/F53xA devices, the startup time is around 350 µs.

UART Pins: <u>The location of the pins used by the serial UART interface is different between</u> <u>C8051F52x/F53x and C8051F52xA/F53xA devices</u>. On C8051F52x/F53x devices, the TX and RX pins used by the UART interface are mapped to the P0.3 (TX) and P0.4 (RX) pins. On C8051F52xA/F53xA, the TX and RX pins used by the UART interface are mapped to the P0.4 (TX) and P0.5 (RX) pins.

Important Note: On C8051F52xA/53xA devices, the UART pins must be skipped if the UART is enabled in order for peripherals to appear on port pins beyond the UART on the crossbar. For example, with the SPI and UART enabled on the crossbar with the SPI on P1.0-P1.3, the UART pins must be skipped using POSKIP for the SPI pins to appear correctly.

LIN: The LIN peripheral behavior in C8051F52x/F53x devices is different than the behavior of C8051F52xA/F53xA devices. The differences are:

Stop Bit Check: On C8051F52x/F53x devices, the stop bits of the fields in the LIN frame are not checked and no error is generated if the stop bits could not be sent or received correctly. On C8051F52xA/F53xA devices, the stop bits are checked, and an error will be generated if the stop bit was not sent or received correctly.

Synch Break and Synch Field Length Check: On C8051F52x/F53x devices, the check of sync field length versus sync break length is incorrect. On C8051F52xA/F53xA devices, the sync break length must be larger than 10 bit times (of the measured bit time) to enable the synchronization.