L99MOD54XP

Multi-output driver for automotive applications

Datasheet - production data

PowerSSO-36

Features

- AEC-Q100 qualified
- Three half bridges for 0.75 A loads (R_{DSon} = 1600 mΩ)
- Two configurable high-side drivers for up to 1.5 A load (R_{DSon} = 500 mΩ) or 0.35 A load (R_{DSon} = 1800 mΩ)
- One high-side driver for 6 A load (R_{DSon} = 100 mΩ)
- Programmable soft start function to drive loads with higher inrush currents (i.e. current > 6 A, current > 1.5 A)
- Very low current consumption in standby mode (I_S < 6 µA typ; $T_j \leq$ 85 °C)
- All outputs short circuit protected
- Current monitor output for high-side OUT1, OUT4, OUT5 and OUT6
- All outputs over temperature protected
- Open-load diagnostic for all outputs
- Overload diagnostic for all outputs
- PWM control of all outputs
- Charge pump output for reverse polarity protection

Applications

L99MOD devices are recommended for those applications that need multiple motors control with additional loads in high-side configuration, such as bulbs/LEDs or requiring protected supply, like sensors or cameras.

Description

The L99MOD54XP is a microcontroller-driven multifunctional actuator driver for automotive applications.

Up to two DC motors and three grounded resistive loads can be driven with three half bridges and three high-side drivers.

The integrated SPI controls all operating modes (forward, reverse, brake and high impedance).

Also all diagnostic information is available via SPI read.

Table 1. Device summary

Package	Order codes	Packing
PowerSSO-36	L99MOD54XPTR	Tape and reel

This is information on a product in full production.

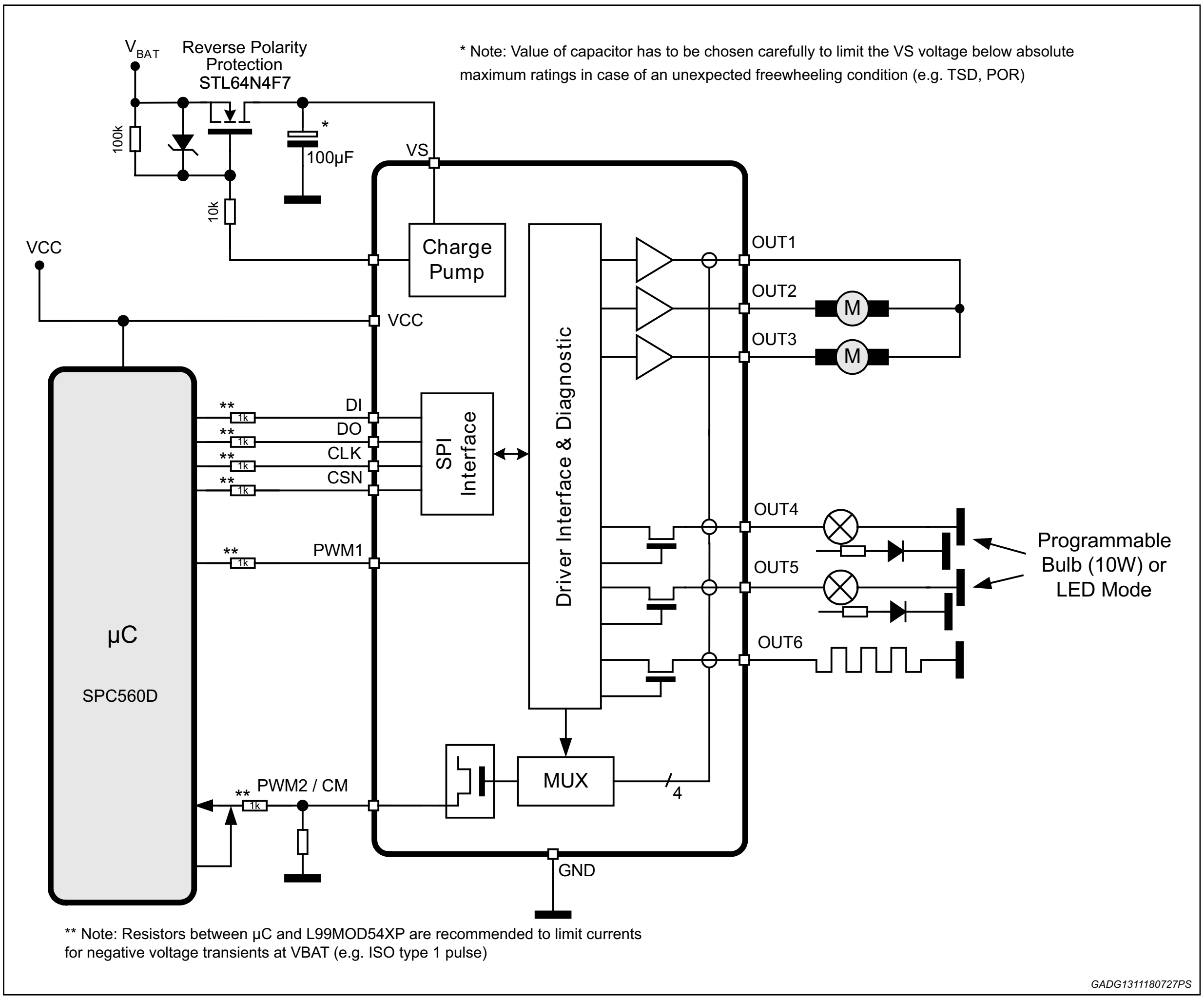
Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram



* Note: Value of capacitor has to be chosen carefully to limit the VS voltage below absolute maximum ratings in case of an unexpected freewheeling condition (e.g. TSD, POR)

** Note: Resistors between µC and L99MOD54XP are recommended to limit currents for negative voltage transients at VBAT (e.g. ISO type 1 pulse)

Figure 2. Configuration diagram (top view)

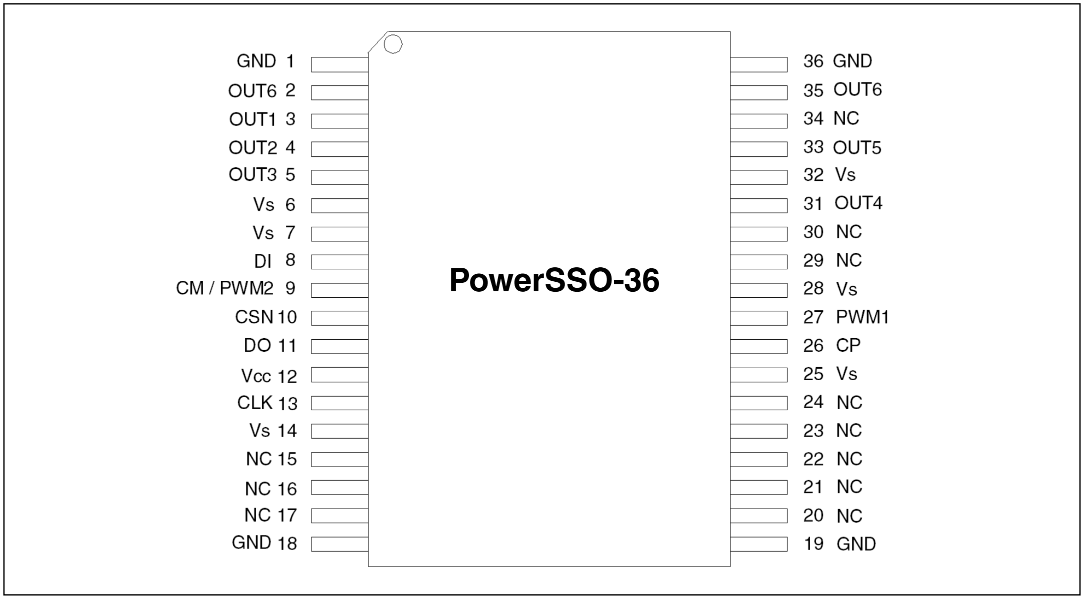


Table 2. Pin definitions and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground: reference potential. Important: for the capability of driving the full current at the outputs all pins of GND must be externally connected.
2, 35	OUT6	High-side driver output 6 The output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to V_S (bulk-drain-diode). The output is over-current and open-load protected. Important: for the capability of driving the full current at the outputs both pins of OUT6 must be externally connected.
3 4 5	OUT1 OUT2 OUT3	Half-bridge output 1,2,3 The output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to V_S, switchs driver from GND to output). This output is over-current and open-load protected.
6, 7, 14, 25, 28, 32	V_S	Power supply voltage (external reverse protection required) For this input a ceramic capacitor as close as possible to GND is recommended. Important: for the capability of driving the full current at the outputs all pins of V_S must be externally connected.
8	DI	Serial data input The input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24bit control word and the least significant bit (LSB, bit 0) is transferred first.

Table 2. Pin definitions and functions (continued)

Pin	Symbol	Function
9	CM/PWM2	Current monitor output/PWM2 input Depending on the selected multiplexer bits of input data register this output sources an image of the instant current through the corresponding high-side driver with a ratio of 1/10.000. This pin is bidirectional. The microcontroller can overdrive the current monitor signal to provide a second PWM input for the output OUT5.
10	CSN	Chip select not input This input is low active and requires CMOS logic levels. The serial data transfer between L99MOD54XP and micro controller is enabled by pulling the input CSN to low-level.
11	DO	Serial data output The diagnosis data is available via the SPI and this 3-state output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high)
12	V_{CC}	Logic supply voltage For this input a ceramic capacitor as close as possible to GND is recommended.
13	CLK	Serial clock input This input controls the internal shift register of the SPI and requires CMOS logic levels.
26	CP	Charge pump output This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection.
27	PWM1	PWM1 input This input signal can be used to control the drivers OUT1-OUT4 and OUT6 by an external PWM signal.
31 33	OUT4, OUT5	High-side driver output 4 and 5 Each output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. Each high-side driver is a power DMOS transistor with an internal parasitic reverse diode from each output to V_S (bulk-drain-diode). Each output is over-current and open-load protected.
15, 16, 17, 20, 21, 22, 23, 24, 29, 30, 34	NC	Not connected pins.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
	Single pulse t_{max} < 400 ms	40	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
V_{DI}, V_{DO}, V_{CLK}, V_{CSN}, V_{pwm1}	Digital input / output voltage	-0.3 to V_{CC} + 0.3	V
V_{CM}	Current monitor output	-0.3 to V_{CC} + 0.3	V
V_{CP}	Charge pump output	-25 to V_S + 11	V
$I_{OUT1,2,3,4,5}$	Output current	±5	A
I_{OUT6}	Output current	±10	A

2.2 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	± 2 (1)	kV
Output pins: OUT1 - OUT6	± 8 (2)	kV

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A.
2. HBM with all unzapped pins grounded.

2.3 Thermal data

Table 5. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

Table 6. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{jTW\ On}$	Temperature warning threshold junction temperature	T_j	130		150	°C
$T_{jSD\ On}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
$T_{jSD\ Off}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
$T_{jSD\ HYS}$	Thermal shutdown hysteresis			5		°K

2.4 Electrical characteristics

Values specified in this section are for V_S = 8 to 16 V, V_{CC} = 4.5 to 5.3 V, T_j = - 40 to 150 °C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 7. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage range		7		28	V
I_S	V_S DC supply current	V_S = 16 V, V_{CC} = 5.3 V active mode OUT1 - OUT6 floating		7	20	mA
	V_S quiescent supply current	V_S = 16 V, V_{CC} = 0 V standby mode OUT1 - OUT6 floating T_{test} = -40 °C, 25 °C		4	12	µA
		T_{test} = 85 °C (1)		6	25	µA
I_{CC}	V_{CC} DC supply current	V_S = 16 V, V_{CC} = 5.3 V CSN = V_{CC} , active mode		1	3	mA
	V_{CC} quiescent supply current	V_S = 16 V, V_{CC} = 5.3 V CSN = V_{CC} standby mode OUT1 - OUT6 floating		25	50	µA
$I_S + I_{CC}$	Sum quiescent supply current	V_S = 16 V, V_{CC} = 5.3 V CSN = V_{CC} standby mode OUT1 - OUT6 floating T_{test} = 130 °C		50	200	µA

1. Guaranteed by design.

Table 8. Overvoltage and under voltage detection

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ On}$	V_S UV-threshold voltage	V_S increasing	5.7		7.2	V
$V_{SUV\ Off}$	V_S UV-threshold voltage	V_S decreasing	5.5		6.9	V

Table 8. Overvoltage and under voltage detection (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ hyst}$	V_S UV-hysteresis	$V_{SUV\ On} - V_{SUV\ Off}$		0.5		V
$V_{SOV\ Off}$	V_S OV-threshold voltage	V_S increasing	18		24.5	V
$V_{SOV\ On}$	V_S OV-threshold voltage	V_S decreasing	17.5		23.5	V
$V_{SOV\ hyst}$	V_S OV-hysteresis	$V_{SOV\ Off} - V_{SOV\ On}$		1		V
$V_{POR\ Off}$	Power-on reset threshold	V_{CC} increasing			4.4	V
$V_{POR\ On}$	Power-on reset threshold	V_{CC} decreasing	3.1			V
$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ Off} - V_{POR\ On}$		0.3		V

Table 9. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CM}	Functional voltage range	$V_{CC} = 5$ V	0		4	V
$I_{CM,r}$	Current monitor output ratio: I_{CM} / I_{OUT6}	$0\ V \leq V_{CM} \leq 4\ V$, $V_{CC} = 5\ V$		$\frac{1}{10000}$		-
	Current monitor output ratio: I_{CM} / I_{OUT1}			$\frac{1}{3800}$		
	Current monitor output ratio: $I_{CM} / I_{OUT4,5}$ low R_{DSon} mode			$\frac{1}{10200}$		
	Current monitor output ratio: $I_{CM} / I_{OUT4,5}$ high R_{DSon} mode			$\frac{1}{2400}$		
$I_{CM\ acc}$	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 8}$	$0\ V \leq V_{CM} \leq 3.8\ V$, $V_{CC} = 5\ V$, $I_{Out,min\ 8} = 0.5\ A$, $I_{Out\ max\ 8} = 5.9\ A$	-8% -2%FS(1)		8% + 2%FS	A
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 1}$	$0\ V \leq V_{CM} \leq 3.8\ V$, $V_{CC} = 5V$, $I_{Out,min\ 1} = 60\ mA$, $I_{Out\ max\ 1} = 0.6\ A$				
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 4,5}$ high R_{DSon} mode	$0\ V \leq V_{CM} \leq 3.8\ V$, $V_{CC} = 5\ V$, $I_{Out,min\ 4,5} = 30\ mA$, $I_{Out\ max\ 4,5} = 300\ mA$				
	Current monitor accuracy Acc $I_{CM} / I_{OUT\ 4,5}$ low R_{DSon} mode	$0\ V \leq V_{CM} \leq 3.8\ V$, $V_{CC} = 5\ V$, $I_{Out,min\ 4,5} = 150\ mA$, $I_{Out\ max\ 4,5} = 1\ A$				

1. FS (full scale)= $I_{OUTmax} * I_{CMr\_typ}$.

Table 10. Charge pump output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 8 V, I_{CP} = -60 µA	V_S+6		V_S+13	V
		V_S = 10 V, I_{CP} = -80 µA	V_S+8		V_S+13	V
		$V_S \geq$ 12 V, I_{CP} = -100 µA	V_S+10		V_S+13	V
I_{CP}	Charge pump output current	V_{CP} = V_S + 10 V, V_S = 13.5 V	95	150	300	µA

Table 11. OUT1 - OUT6

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DSon\ OUT1}$, $R_{DSon\ OUT2}$ $R_{DSon\ OUT3}$	On resistance to supply or GND	V_S = 13.5 V, T_j = 25 °C, $I_{OUT1,2,3}$ = ± 0.4 A		1600	2200	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT1,2,3}$ = ± 0.4 A		2500	3400	mΩ
$R_{DSon\ OUT4}$, $R_{DSon\ OUT5}$	On resistance to supply in low R_{DSon} mode	V_S = 13.5 V, T_j = 25 °C, $I_{OUT4,5}$ = -0.8 A		500	700	mΩ
		V_S = 13.5 V, T_j = 125 °C, $I_{OUT4,5}$ = -0.8 A		700	950	mΩ
	On resistance in high R_{DSon} mode	T_j = 25 °C, $I_{OUT4,5}$ = - 0.2 A		2000	2700	mΩ
		T_j = 125 °C, $I_{OUT4,5}$ = - 0.2 A		3200	4300	mΩ
$R_{DSon\ OUT6}$	On resistance to supply	V_S = 13.5 V, T_j = 25 °C, I_{OUT6} = –3 A		100	150	mΩ
		V_S = 13.5 V, T_j = 125 °C, I_{OUT6} = –3 A		150	200	mΩ
I_{OUT1} I_{OUT2} I_{OUT3}	Output current limitation to GND	Source, V_S = 13.5 V	-1.25		-0.75	A
I_{OUT1} I_{OUT2} I_{OUT3}	Output current limitation to supply	Sink, V_S = 13.5 V	0.75		1.25	A
I_{OUT4} I_{OUT5}	Output current limitation to GND in low R_{DSon} mode	Source, V_S = 13.5 V	-3.0		-1.5	A
	Output current limitation to GND in high R_{DSon} mode		-0.65		-0.35	A
I_{OUT6}	Output current limitation to GND	Source, V_S = 13.5 V	-10.5		-6	A
$t_{d\ On\ H}$	Output delay time, high-side driver on	V_S = 13.5 V, R_{load} = (1) corresponding low-side driver is not active	10	40	80	µs
$t_{d\ Off\ H}$	Output delay time, high-side driver off	V_S = 13.5 V, R_{load} = (2)	15	150	300	µs

Table 11. OUT1 - OUT6 (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ On\ L}$	Output delay time, low-side driver on	V_S = 13.5 V, R_{load} = (2) corresponding high-side driver is not active	15	30	70	µs
$t_{d\ Off\ L}$	Output delay time, low-side driver off	V_S = 13.5 V, R_{load} = (2)	20	150	300	µs
$t_{d\ HL}$	Cross current protection time, source to sink	$t_{CC\ ONLS\_OFFHS}$ - $t_{d\ Off\ H}$(2)		200	400	µs
$t_{d\ LH}$	Cross current protection time, sink to source	$t_{CC\ ONHS\_OFFLS}$ - $t_{d\ OFF\ L}$(2)		200	400	µs
I_{QLH}	Switched-off output current high-side drivers of OUT1-6	$V_{OUT1\text{-}6}$ = 0 V, standby mode	-3	0	-3	µA
		$V_{OUT1\text{-}2\text{-}3\text{-}6}$ = 0 V, active mode	-40	-15	0	µA
		$V_{OUT4\text{-}5}$ = 0 V, active mode	-10	-8	0	µA
I_{QLL}	Switched-off output current low-side drivers of OUT1-3	$V_{OUT1\text{-}3}$ = V_S, standby mode	0	80	120	µA
		$V_{OUT1\text{-}3}$ = V_S, active mode	-40	-15	0	µA
I_{OLD123}	Open-load detection current of OUT1, OUT2 and OUT3	Source and sink	10	20	30	mA
I_{OLD45}	Open-load detection current of OUT4 and OUT5	Source	15	40	60	mA
	Open-load detection current of OUT4 and OUT5 in high R_{DSon} mode		5	10	15	mA
I_{OLD6}	Open-load detection current of OUT6	Source	30	150	300	mA
$t_{d\ OL}$	Minimum duration of open-load condition to set the status bit		500		3000	µs
t_{ISC}	Minimum duration of over-current condition to switch off the driver		10		100	µs
f_{rec0}	Recovery frequency for OC recovery duty cycle bit=0		1		4	kHz
f_{rec1}	Recovery frequency for OC recovery duty cycle bit=1		2		6	kHz
dV_{OUT123}/dt dV_{OUT45}/dt	Slew rate of OUT_{123} and OUT_{45}	V_S = 13.5 V, R_{load} = (2)	0.1	0.4	0.9	V/µs
dV_{OUT6}/dt	Slew rate of OUT_6	V_S = 13.5 V, R_{load} = (2)	0.08	0.2	0.4	V/µs

1. OUT1,2,3 32 Ω
   OUT4,5 16 Ω
   OUT4,5 high RDSon mode 63 Ω
   OUT6 4 Ω

2. $t_{CC\ ON}$ is the switch On delay time $t_{d\ ON}$ if complement in half bridge has to switch off.

2.5 SPI - electrical characteristics

Values specified in this section are V_S = 8 to 16 V, V_{CC} = 4.5 to 5.3 V, T_j = - 40 to 150 °C, unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 12. Delay time from standby to active mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{set}	Delay time	Switching from standby to active mode. Time until output drivers are enabled after CSN going to high.		160	300	µs

Table 13. Inputs: CSN, CLK, PWM1/2 and DI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{inL}	Input low-level	V_{CC} = 5 V	1.5	2.0		V
V_{inH}	Input high-level	V_{CC} = 5 V		3.0	3.5	V
V_{inHyst}	Input hysteresis	V_{CC} = 5 V	0.5			V
$I_{CSN\ in}$	Pull up current at input CSN	V_{CSN} = 3.5 V, V_{CC} = 5 V	-40	-20	-5	µA
$I_{CLK\ in}$	Pull down current at input CLK	V_{CLK} = 1.5 V	10	25	50	µA
$I_{DI\ in}$	Pull down current at input DI	V_{DI} = 1.5 V	10	25	50	µA
$I_{PWM1\ in}$	Pull down current at input PWM1	V_{PWM} = 1.5 V	10	25	50	µA
C_{in}(1)	Input capacitance at input CSN, CLK, DI and PWM1/2	0 V < V_{CC} < 5.3 V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 14. DI timing

Symbol	Parameter(1)	Test condition	Min.	Typ.	Max.	Unit
t_{CLK}	Clock period	V_{CC} = 5 V	1000	-		ns
t_{CLKH}	Clock high time	V_{CC} = 5 V	400	-		ns
t_{CLKL}	Clock low time	V_{CC} = 5 V	400	-		ns
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V_{CC} = 5 V	400	-		ns
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V_{CC} = 5 V	400	-		ns
$t_{set\ DI}$	DI setup time	V_{CC} = 5 V	200	-		ns
$t_{hold\ DI}$	DI hold time	V_{CC} = 5 V	200	-		ns

Table 14. DI timing (continued)

Symbol	Parameter[1]	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ in}$	Rise time of input signal DI, CLK, CSN	V_{CC} = 5 V		-	100	ns
$t_{f\ in}$	Fall time of input signal DI, CLK, CSN	V_{CC} = 5 V		-	100	ns

1. DI timing parameters tested in production by a passed / failed test:
Tj = -40 °C / +25 °C: SPI communication @ 2 MHz.
Tj = +125 °C SPI communication @ 1.25 MHz.

Table 15. DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DOL}	Output low-level	V_{CC} = 5 V, I_D = -2 mA		0.2	0.4	V
V_{DOH}	Output high-level	V_{CC} = 5 V, I_D = 2 mA	V_{CC} - 0.4	V_{CC} - 0.2		V
I_{DOLK}	3-state leakage current	V_{CSN} = V_{CC}, 0V < V_{DO} < V_{CC}	-10		10	µA
C_{DO} (1)	3-state input capacitance	V_{CSN} = V_{CC}, 0 V < V_{CC} < 5.3 V		10	15	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

Table 16. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_L = 100 pF, I_{load} = -1 mA	-	80	140	ns
$t_{f\ DO}$	DO fall time	C_L = 100 pF, I_{load} = 1 mA	-	50	100	ns
$t_{en\ DO\ tri\ L}$	DO enable time from 3-state to low-level	C_L = 100 pF, I_{load} = 1 mA pull up load to V_{CC}	-	100	250	ns
$t_{dis\ DO\ L\ tri}$	DO disable time from low-level to 3-state	C_L = 100 pF, I_{load} = 4 mA pull up load to V_{CC}	-	380	450	ns
$t_{en\ DO\ tri\ H}$	DO enable time from 3-state to high-level	C_L =100 pF, I_{load} = -1 mA pull down load to GND	-	100	250	ns
$t_{dis\ DO\ H\ tri}$	DO disable time from high-level to 3-state	C_L = 100 pF, I_{load} = -4 mA pull down load to GND	-	380	450	ns
$t_{d\ DO}$	DO delay time	V_{DO} < 0.3 V_{CC}, V_{DO} > 0.7 V_{CC}, C_L = 100pF	-	50	250	ns

Table 17. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{CSN\_HI,stb}$	CSN HI time, switching from standby mode	Transfer of SPI command to Input Register	20	-	-	µs
$t_{CSN\_HI,min}$	CSN HI time, active mode	Transfer of SPI command to input register	4	-	-	µs

Figure 3. SPI - transfer timing diagram

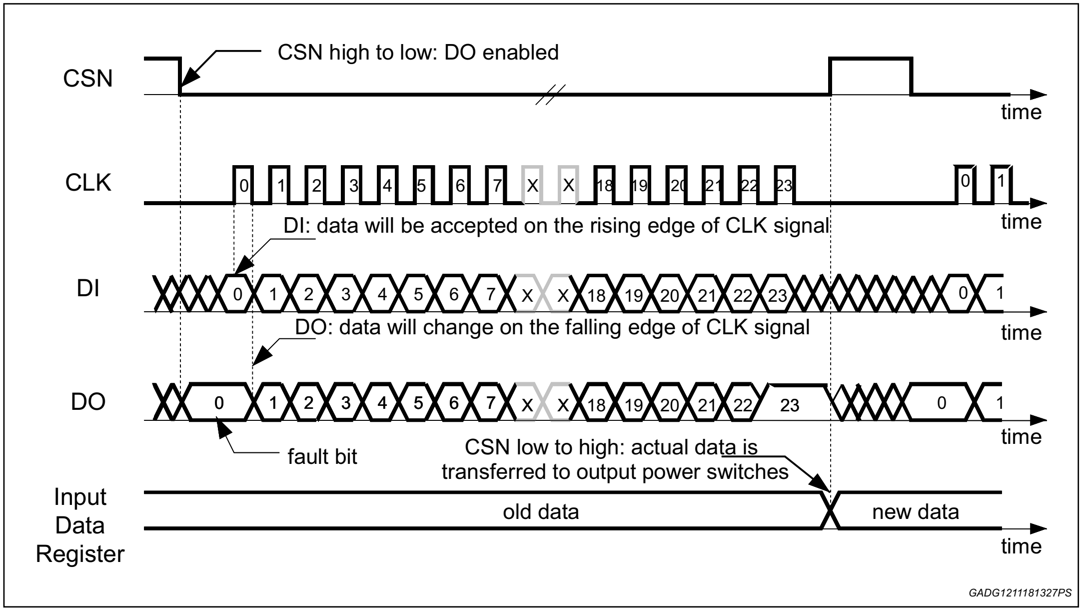


Figure 4. SPI - input timing

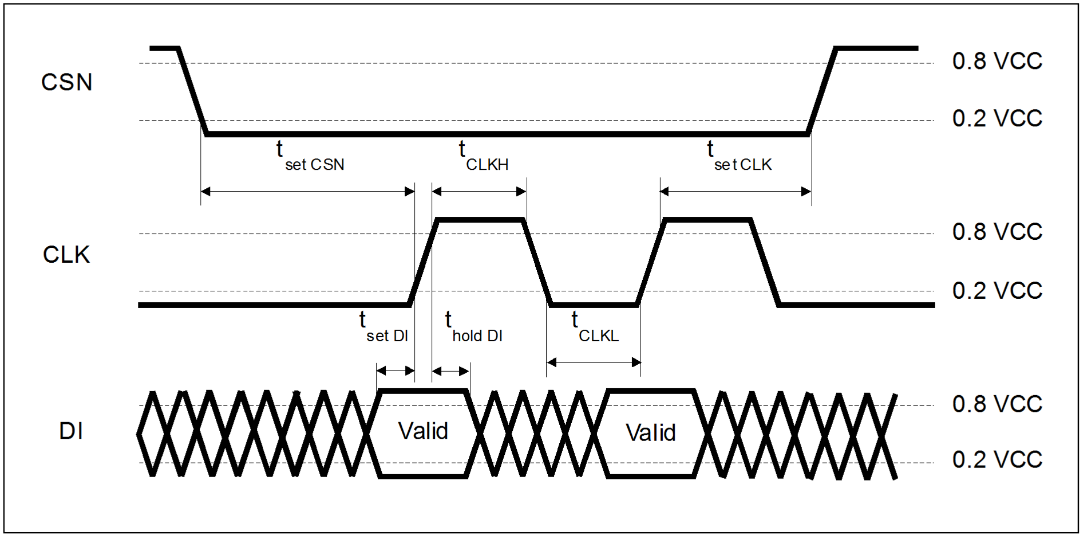


Figure 5. SPI - DO valid data delay time and valid time

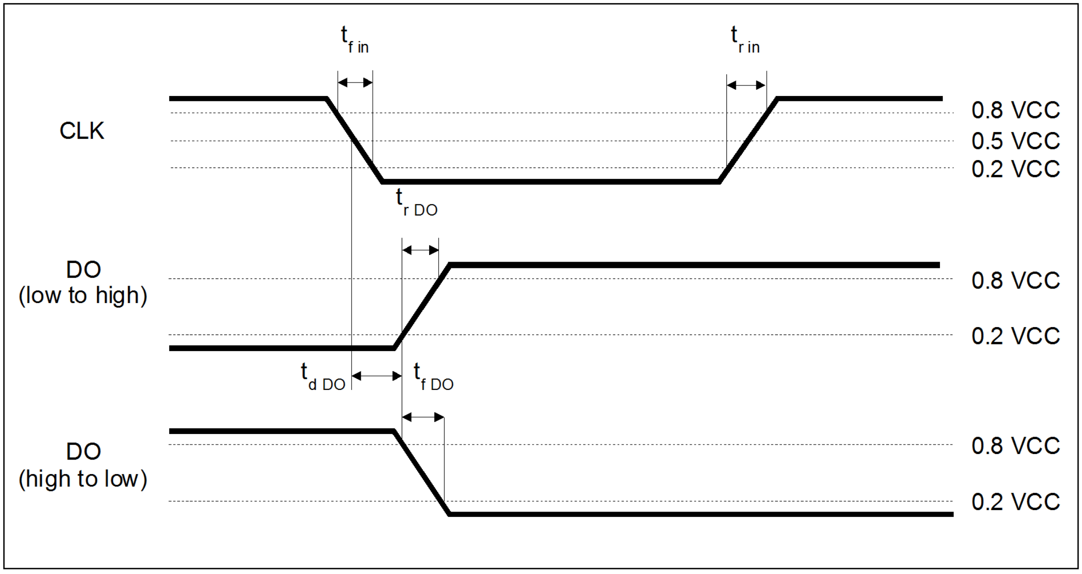


Figure 6. SPI - DO enable and disable time

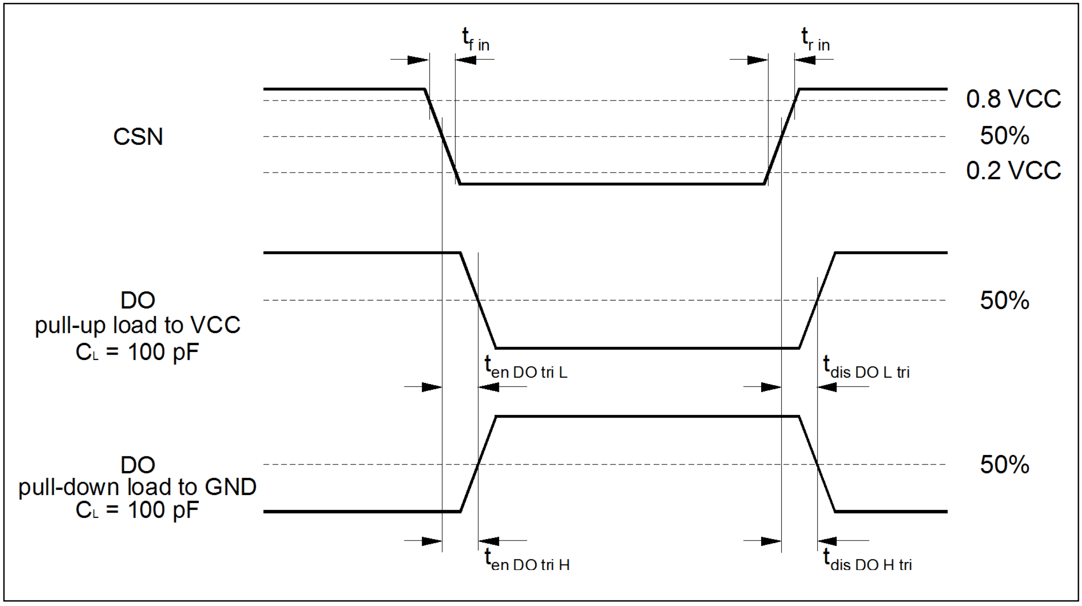


Figure 7. SPI - driver turn-on / off timing, minimum CSN HI time

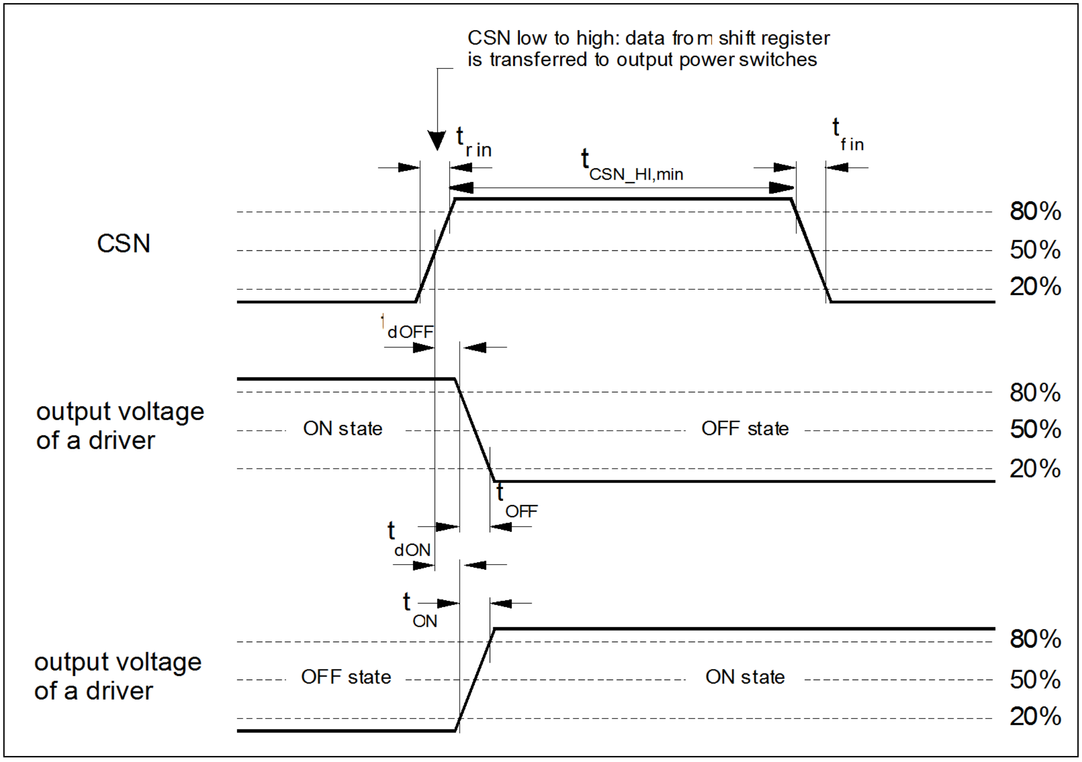
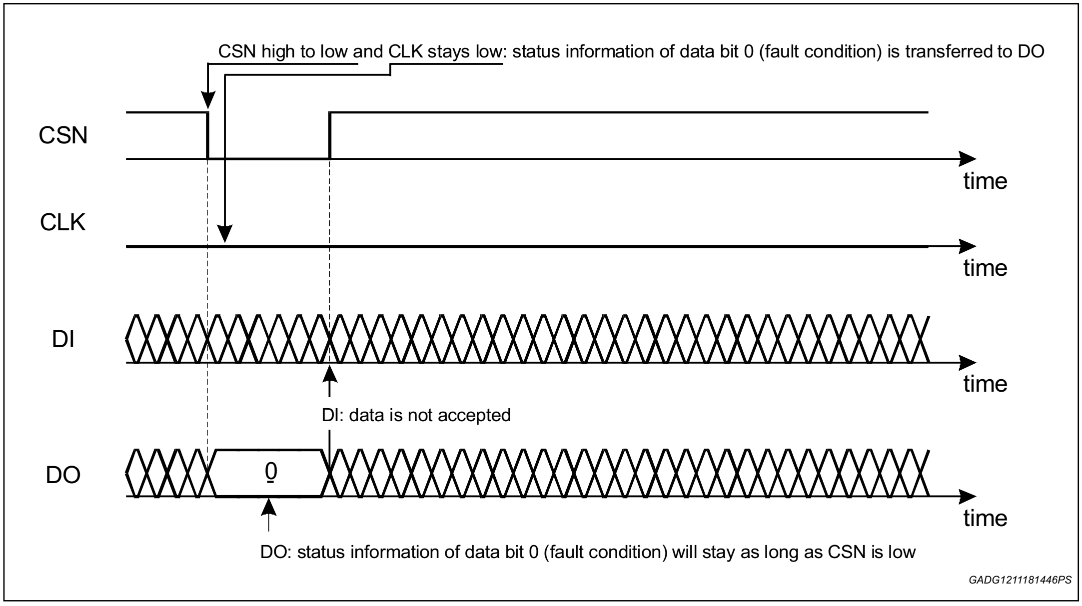


Figure 8. SPI - timing of status bit 0 (fault condition)



3 Application information

3.1 Dual power supply: V_S and V_{CC}

The power supply voltage V_S supplies the half bridges and the high-side drivers. An internal charge-pump is used to drive the high-side switches. The logic supply voltage V_{CC} (stabilized 5 V) is used for the logic part and the SPI of the device.

Due to the independent logic supply voltage the control and status information is not lost, if there are temporary spikes or glitches on the power supply voltage. In case of power-on (V_{CC} increases from under voltage to $V_{POR\ Off}$ = 4.2 V) the circuit is initialized by an internally generated power-on-reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 3.4 V), the outputs are switched to 3-state (high impedance) and the status registers are cleared.

3.2 Standby mode

The standby mode of the L99MOD54XP is activated by clearing the bit 23 of the input data register 0. All latched data is cleared and the inputs and outputs are switched to high impedance. In the standby mode the current at V_S (V_{CC}) is less than 6 µA (50µA) for CSN = high (DO in 3-state). By switching the V_{CC} voltage a very low quiescent current can be achieved. If bit 23 is set, the device is switched to active mode.

3.3 Inductive loads

Each half bridge is built by an internally connected high-side and a low-side power DMOS transistor. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT3 without external free-wheeling diodes. The high-side drivers OUT4 to OUT6 are intended to drive resistive loads. Hence only a limited energy (E<1mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L>100µH) an external free-wheeling diode connected to GND and the corresponding output is needed.

3.4 Diagnostic functions

All diagnostic functions (over/open-load, power supply over-/under voltage, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 32 µs (open-load: 1 ms, respectively) before the corresponding status bit in the status registers is set. The filters are used to improve the noise immunity of the device. Open-load and temperature warning functions are intended for information purpose and don't change the state of the output drivers. On the contrary, the overload condition disables the corresponding driver (over-current) and overtemperature switches off all drivers (thermal shutdown). Without setting the over-current recovery bits in the input data register, the microcontroller has to clear the over-current status bits to reactivate the corresponding drivers.

3.5 Overvoltage and under voltage detection

If the power supply voltage V_S rises above the overvoltage threshold $V_{SOV\ Off}$ (typical 21 V), the outputs OUT1 to OUT6 are switched to high impedance state to protect the load. When the voltage V_S drops below the under voltage threshold $V_{SUV\ Off}$ (UV-switch-off voltage), the output stages are switched to the high impedance to avoid the operation of the power devices without sufficient gate driving voltage (increased power dissipation). If the supply voltage V_S recovers (register 0: bit 20=0) to normal operating voltage the outputs stages return to the programmed state after at least 32 µs.

If the under voltage/overvoltage recovery disable bit is set, the automatic turn-on of the drivers is deactivated. The microcontroller needs to clear the status bits to reactivate the drivers. It is strongly recommended to set bit 20 to avoid a possible high current oscillation in case of a shorted output to GND and low battery voltage.

3.6 Charge pump

The charge pump runs under all conditions in normal mode. In standby the charge pump is out of action.

3.7 Temperature warning and thermal shutdown

If junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set after at least 32 µs and is detectable via the SPI. If junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit is set and power DMOS transistors of all output stages are switched off to protect the device after at least 32 µs. Temperature warning flag and thermal shutdown bit are latched and must be cleared by the microcontroller. The related bit is only cleared if the temperature decreases below the trigger temperature. If the thermal shutdown bit has been cleared the output stages are reactivated.

3.8 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least 1 ms (t_{dOL}) the corresponding open-load bit is set in the status register. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical/electrical state of the loads.

3.9 Overload detection

In case of an over-current condition a flag is set in the status register in the same way as open-load detection. If the over-current signal is valid for at least t_{ISC} = 32 µs, the over-current flag is set and the corresponding driver is switched off to reduce the power dissipation and to protect the integrated circuit. If the over-current recovery bit of the output is zero the microcontroller has to clear the status bits to reactivate the corresponding driver.

3.10 Current monitor

The current monitor output sources a current image at the current monitor output which has a fixed ratio (1/10000) of the instantaneous current of the selected high-side driver. Signal at output CM is blanked after switching on of driver until correct settlement of circuitry (at least for 32 µs).

The bits 18 and 19 of the input data register 0 control which of the outputs OUT1, OUT4, OUT5 and OUT6 is multiplexed to the current monitor output. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open- or overload condition. For example this can be used to detect the motor state (starting, free-running, stalled). Moreover, it is possible to regulate the power of the defroster more precisely by measuring the load current. The current monitor output is bidirectional (c.f. PWM inputs).

3.11 PWM inputs

Each driver has a corresponding PWM enable bit which can be programmed by the SPI interface. If the PWM enable bit in Input data register 1 is set, the output is controlled by the logically AND-combination of the PWM signal and the output control bit in input data register 0. The outputs OUT1-OUT4 and OUT6 are controlled by the PWM1 input and the output OUT5 is controlled by the bidirectional input CM/PMW2. For example, the two PWM inputs can be used to dim two lamps independently by external PWM signals.

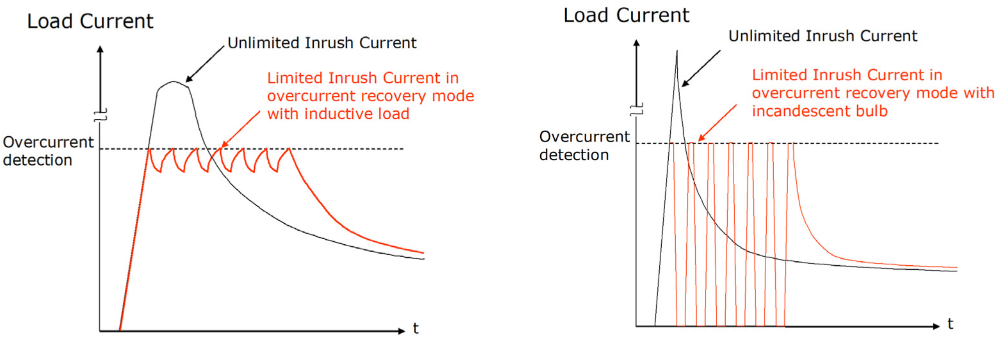
3.12 Cross-current protection

The three half-bridges of the device are cross-current protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge is automatically delayed by the cross-current protection time. After the cross-current protection time is expired the slew-rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver starts to conduct.

3.13 Programmable soft start function to drive loads with higher inrush current

Loads with start-up currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable soft start function (i.e. overcurrent recovery mode). Each driver has a corresponding over-current recovery bit. If this bit is set, the device switches-on automatically the outputs again after a programmable recovery time. The duty cycle in over-current condition can be programmed by the SPI interface to be about 15 %...25 %. The PWM modulated current provides sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.5 kHz or 3 kHz. The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch on light bulbs by setting the over-current recovery bit for the first 50ms. After clearing the recovery bit the output is automatically disabled if the overload condition still exits.

Figure 9. Programmable soft start function for inductive loads and incandescent bulbs



4 Functional description of the SPI

4.1 Serial Peripheral Interface (SPI)

This device uses a standard SPI to communicate with a microcontroller. The SPI can be driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin reflects the status bit 0 (fault condition) of the device which is a logical-or of all bits in the status registers 0 and 1. The microcontroller can poll the status of the device without the need of a full SPI communication cycle.

Note: In contrast to the SPI standard the least significant bit (LSB) is transferred first (see Figure 3).

4.2 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state when CSN is going low until the rising edge of CSN is called a communication frame.

Note: The device includes a test mode. This mode is activated by a dedicated sequence which includes a high voltage at the CSN pin. The CSN pin must be kept at nominal voltage levels in order to avoid accidental activation of the test mode.

4.3 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 24-bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to data input register. The writing to the selected data input register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

4.4 Serial Data Out (DO)

The data output driver is activated by a logical low-level at the CSN input and goes from high impedance to a low or high-level depending on the status bit 0 (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

4.5 Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal.

4.6 Input Data Register

The device has two input registers. The first bit (bit 0) at the DI input is used to select one of the two input registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register is written to the selected input data register only if a frame of exact 24 data bits is detected. Depending on bit 0 the content of the selected status register is transferred to DO during the current communication frame. Bit 1-17 controls the behavior of the corresponding driver.

If bit 23 is zero, the device goes into the standby mode. The bits 18 and 19 are used to control the current monitor multiplexer. Bit 22 is used to reset all status bits in both status registers. The bits in the status registers are cleared after the current communication frame (rising edge of CSN).

4.7 Status register

This device uses two status registers to store and to monitor the state of the device. No error bit (bit 0) is used as a fault bit and is a logical-NOR combination of bits 1-22 in both status registers. The state of this bit can be polled by the microcontroller without the need of a full SPI communication cycle. If one of the over-current bits is set, the corresponding driver is disabled. If the over-current recovery bit of the output is not set the microcontroller has to clear the over-current bit to enable the driver. If the thermal shutdown bit is set, all drivers go into a high impedance state. Again the microcontroller has to clear the bit to enable the drivers.

4.8 SPI - input data and status registers

Table 18. SPI - input data and status registers 0

<table>
<tr><th rowspan="2">Bit</th><th colspan="5">Input register 0 (write)</th><th colspan="2">Status register 0 (read)</th></tr>
<tr><th colspan="2">Name</th><th colspan="3">Comment</th><th>Name</th><th>Comment</th></tr>
<tr><td>23</td><td colspan="2">Enable bit</td><td colspan="3">If enable bit is set the device switches in active mode. If enable bit is cleared the device goes into standby mode and all bits are cleared. After power-on reset device starts in standby mode.</td><td>Always 1</td><td>A broken V_{CC}-or SPI connection of the L99MOD54XP can be detected by the microcontroller, because all 24 bits low or high is not a valid frame.</td></tr>
<tr><td>22</td><td colspan="2">Reset bit</td><td colspan="3">If reset bit is set both status registers are cleared after rising edge of CSN input.</td><td>V_S overvoltage</td><td rowspan="3">In case of an overvoltage or undervoltage event the corresponding bit is set and the outputs are deactivated. If V_S voltage recovers to normal operating conditions outputs are reactivated automatically (if bit 20 of status register 0 is not set).</td></tr>
<tr><td rowspan="2">21</td><td colspan="2">OC recovery duty cycle</td><td colspan="3" rowspan="2">This bit defines in combination with the over-current recovery bit (input register 1) the duty cycle in overcurrent condition of an activated driver.</td><td rowspan="2">V_S undervoltage</td></tr>
<tr><td>0: 12%</td><td>1: 25%</td></tr>
<tr><td>20</td><td colspan="2">Overvoltage/ undervoltage recovery disable</td><td colspan="3">If this bit is set the microcontroller has to clear the status register after under voltage / overvoltage event to enable the outputs.</td><td>Thermal shutdown</td><td>In case of a thermal shutdown all outputs are switched off.
The microcontroller has to clear the TSD bit by setting the Reset Bit to reactivate the outputs.</td></tr>
<tr><td>19</td><td colspan="2" rowspan="7">Current monitor select bits</td><td colspan="3">Depending on combination of bit 18 and 19 the current image (1/10.000) of the selected HS-output is multiplexed to the CM output:</td><td>Temperature warning</td><td>The TW bit can be used for thermal management by the microcontroller to avoid a thermal shutdown. The microcontroller has to clear the TW bit.</td></tr>
<tr><td rowspan="6">18</td><td>Bit 19</td><td>Bit 18</td><td>Output</td><td rowspan="6">Not ready bit</td><td rowspan="6">After switching the device from standby mode to active mode an internal timer is started to allow charge pump to settle before the outputs can be activated. This bit is cleared automatically after start up time has finished. Since this bit is controlled by internal clock it can be used for synchronizing testing events (e.g. measuring filter times).</td></tr>
<tr><td>0</td><td>0</td><td>OUT6</td></tr>
<tr><td>1</td><td>0</td><td>OUT1</td></tr>
<tr><td>0</td><td>1</td><td>OUT4</td></tr>
<tr><td>1</td><td>1</td><td>OUT5</td></tr>
<tr><td colspan="3"></td></tr>
</table>

Table 18. SPI - input data and status registers 0 (continued)

Bit	Input register 0 (write)		Status register 0 (read)	
	Name	Comment	Name	Comment
17	OUT6 – HS on/off	If a bit is set the selected output driver is switched on. If the corresponding PWM enable bit is set (input register 1) the driver is only activated if PWM1 (PWM2) input signal is high. The outputs of OUT1-OUT3 are half bridges. If the bits of HS- and LS-driver of the same half bridge are set, the internal logic prevents that both drivers of this output stage can be switched on simultaneously in order to avoid a high internal current from V_S to GND.	OUT6 – HS over-current	In case of an over-current event the corresponding status bit is set and the output driver is disabled. If the over-current recovery enable bit is set (input register 1) the output is automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 21). If the over-current recovery bit is not set the microcontroller has to clear the over-current bit (reset bit) to reactivate the output driver.
16	x (don’t care)		0	
15	OUT5 – HS on/off		OUT5 – HS over-current	
14	OUT4 – HS on/off		OUT4 – HS over-current	
13	x (don’t care)		0	
12	x (don’t care)		0	
11	x (don’t care)		0	
10	x (don’t care)		0	
9	x (don’t care)		0	
8	x (don’t care)		0	
7	x (don’t care)		0	
6	OUT3 – HS on/off		OUT3 – HS over-current	
5	OUT3 – LS on/off		OUT3 – LS over-current	
4	OUT2 – HS on/off		OUT2 – HS over-current	
3	OUT2 – LS on/off		OUT2 – LS over-current	
2	OUT1 – HS on/off		OUT1 – HS over-current	
1	OUT1 – LS on/off		OUT1 – LS over-current	
0	0		No error bit	A logical NOR-combination of all bits 1 to 22 in both status registers.

Table 19. SPI - input data and status registers 1

Bit	Input register 1 (write)		Status register 1 (read)	
	Name	Comment	Name	Comment
23	Enable bit	If enable bit is set the device is switched in active mode. If enable bit is cleared device goes into standby mode and all bits are cleared. After power-on reset device starts in standby mode.	Always 1	A broken V_{CC} or SPI connection of the L99MOD54XP can be detected by the microcontroller, because all 24 bits low or high is not a valid frame.
22	OUT6 OC recovery enable	In case of an over-current event the over-current status bit (status register 0) is set and the output is switched off. If the over current recovery enable bit is set the output is automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle (bit 21 of input data register 0). Depending on occurrence of overcurrent event and internal clock phase it is possible that one recovery cycle is executed even if this bit is set to zero.	V_S overvoltage	In case of an overvoltage or under voltage event the corresponding bit is set and the outputs are deactivated. If V_S voltage recovers to normal operating conditions outputs are reactivated automatically.
21	x (don't care)		V_S undervoltage	
20	OUT5 OC recovery enable		Thermal shutdown	In case of a thermal shutdown all outputs are switched off. The microcontroller has to clear the TSD bit by setting the reset bit to reactivate the outputs.
19	OUT4 OC recovery enable		Temperature warning	The TW bit can be used for thermal management by the microcontroller to avoid a thermal shutdown. The microcontroller has to clear the TW bit.
18	x (don't care)		Not ready bit	After switching the device from standby mode to active mode an internal timer is started to allow charge pump to settle before the outputs can be activated. This bit is only present during start up time. Since this bit is controlled by internal clock it can be used for synchronizing testing events(e.g. measuring filter times).

Table 19. SPI - input data and status registers 1 (continued)

Bit	Input register 1 (write)		Status register 1 (read)	
	Name	Comment	Name	Comment
17	Enable high R_{DSon} OUT5	After 50ms the bit can be cleared. If over-current condition still exists, a wrong load can be assumed.	OUT6 – HS open-load	The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least 1 ms (t_{dOL}) the corresponding open-load bit is set. Due to mechanical/electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical/electrical state of the loads.
16	x (don’t care)		0	
15	x (don’t care)		OUT5 – HS open-load	
14	OUT3 OC recovery enable		OUT4 – HS open-load	
13	OUT2 OC recovery enable		0	
12	OUT1 OC recovery enable		0	
11	OUT6 PWM1 enable	If the PWM1/2 enable bit is set and the output is enabled (input register 0) the output is switched on if PWM1/2 input is high and switched off if PWM1/2 input is low. OUT5 is controlled by PWM2 input. All other outputs are controlled by PWM1 input.	0	
10	x (don’t care)		0	
9	OUT5 PWM2 enable		0	
8	OUT4 PWM1 enable		0	
7	x (don’t care)		0	
6	Enable high R_{DSon} OUT4		OUT3 – HS open-load	
5	x (don’t care)		OUT3 – LS open-load	
4	x (don’t care)		OUT2 –HS open-load	
3	OUT3 PWM1 enable		OUT2– LS open-load	
2	OUT2 PWM1 enable		OUT1 – HS open-load	
1	OUT1 PWM1 enable		OUT1 – LS open-load	
0	1		No error bit	A logical NOR-combination of all bits 1 to 22 in both status registers.

5 Package and PCB thermal data

5.1 PowerSSO-36 thermal data

Figure 10. PowerSSO-36 2 layer PCB

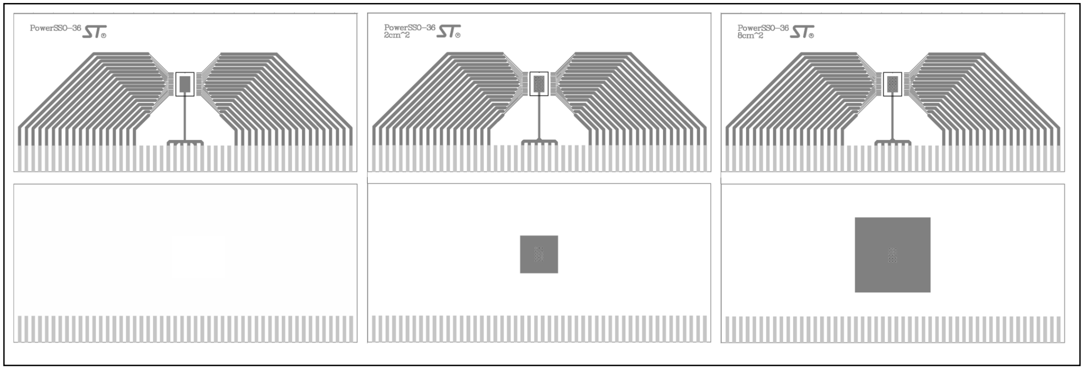
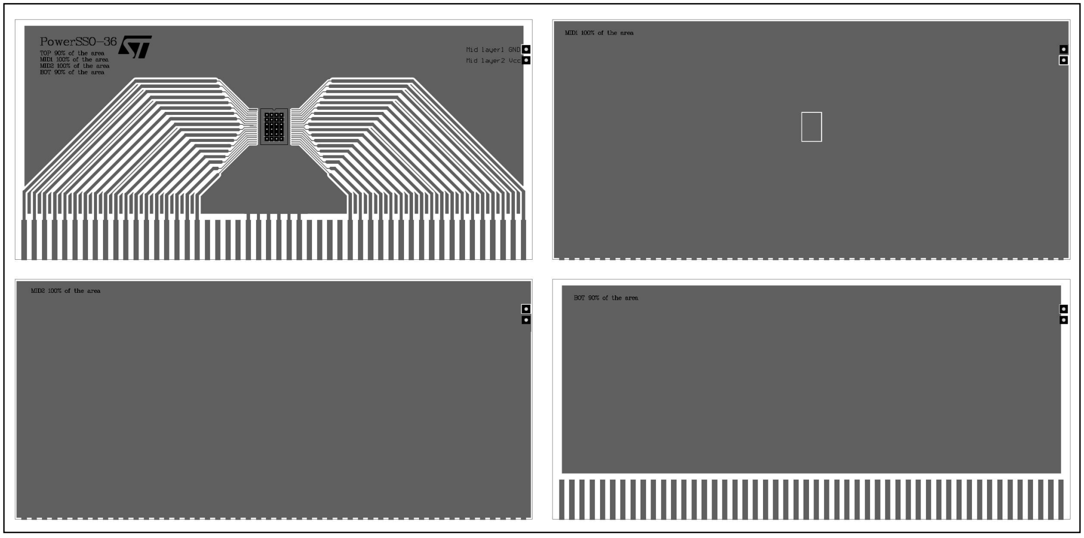
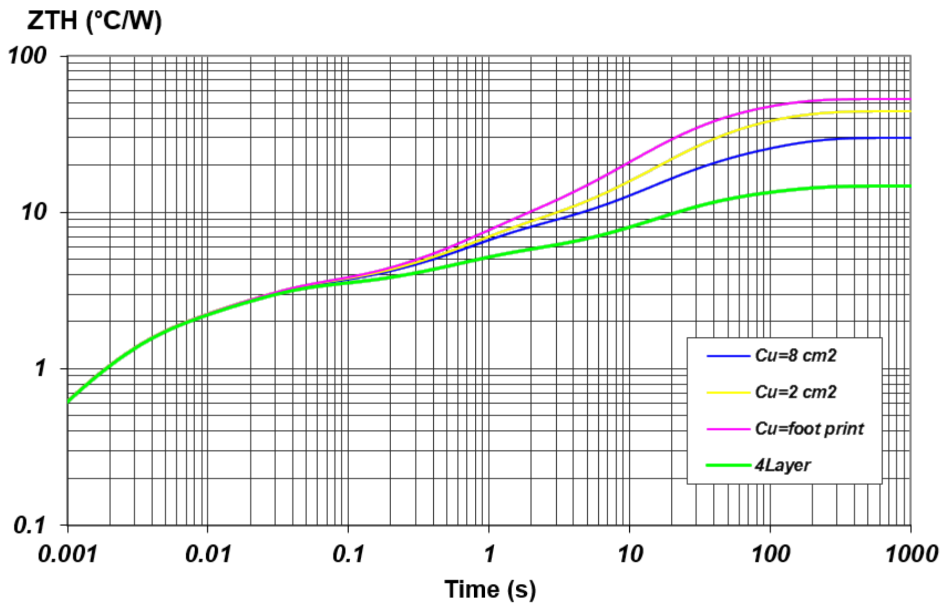


Figure 11. PowerSSO-36 4 layer PCB



Note: *Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm ±10%, board double layer and four layers, board dimension 129 mm x 60 mm, board material FR4, Cu thickness 0.070 mm (outer layers), Cu thickness 0.035 mm (inner layers), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm, Cu thickness on vias 0.025 mm, footprint dimension 4.1 mm x 6.5 mm). 4-layer PCB: Cu on mid1 and mid2 layer: 76.45 cm^2. Cu on bottom layer: 68.8 cm^2. Z_{th} measured on the major power dissipator contributor.*

Figure 12. PowerSSO-36 thermal impedance junction to ambient vs PCB copper area



6 Package and packing information

6.1 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.2 PowerSSO-36 package information

Figure 13. PowerSSO-36 package dimensions

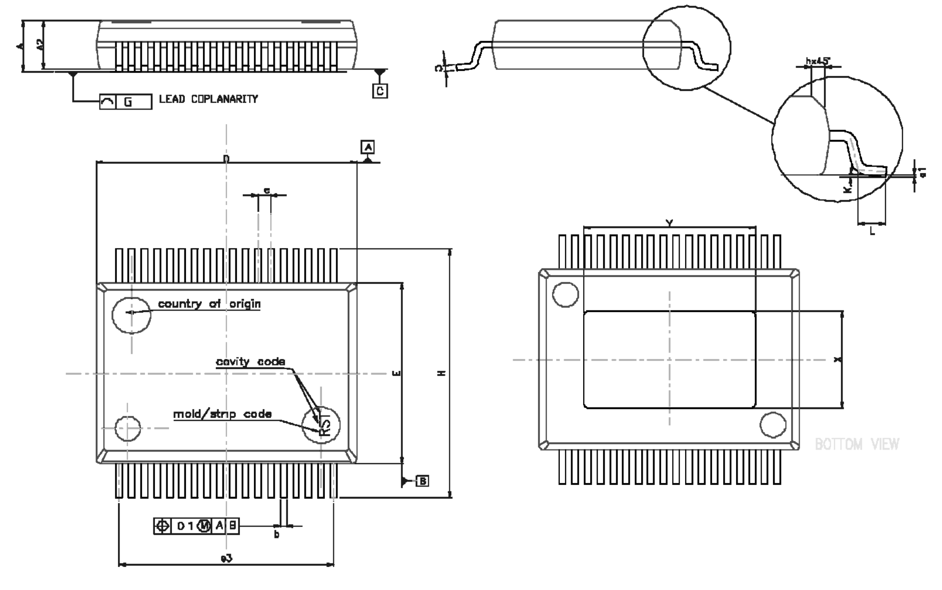


Table 20. PowerSSO-36 mechanical data

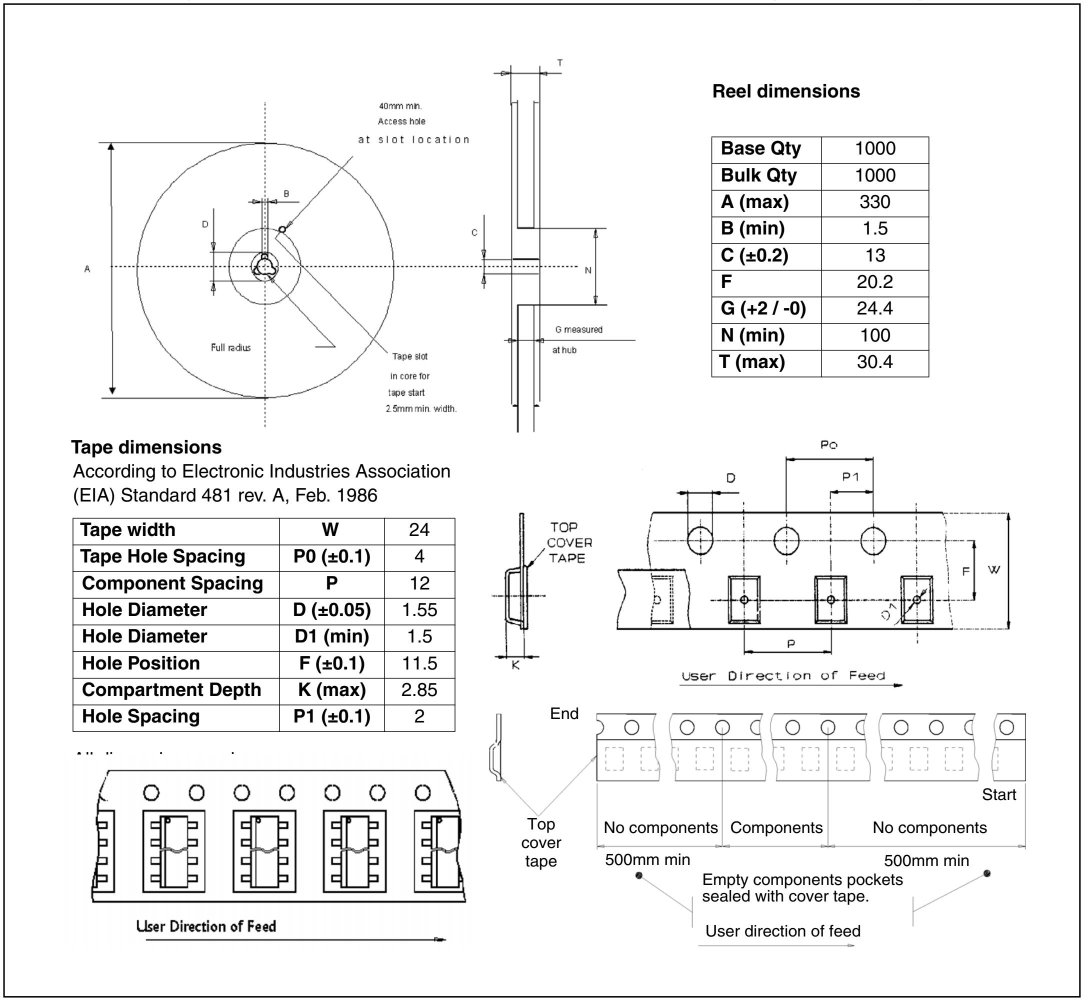
Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.47
A2	2.15	-	2.40
a1	0	-	0.075
b	0.18	-	0.36
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.5	-

Table 20. PowerSSO-36 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
e3	-	8.5	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10 deg
X	4.3	-	5.2
Y	6.9	-	7.5

6.3 PowerSSO-36 packing information

Figure 14. PowerSSO-36 tape and reel shipment (suffix “TR”)



Reel dimensions

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (±0.1)**	2

7 Revision history

Table 21. Document revision history

Date	Revision	Changes
24-Jul-2018	1	Initial release.
09-Nov-2018	2	Added *Section 5: Package and PCB thermal data*.
13-Jun-2019	3	Updated the maturity from target specification to production data.
08-Oct-2019	4	Updated *Applications* on cover page. Updated *Section 4.2: Chip Select Not (CSN)*. Minor text changes

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