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August 2016

# FCB110N65F

## N-Channel SuperFET® II FRFET® MOSFET

650 V, 35 A, 110 mΩ

### Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 96\text{ m}\Omega$  (Typ.)
- Ultra Low Gate Charge (Typ.  $Q_g = 98\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 464\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

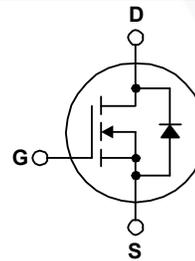
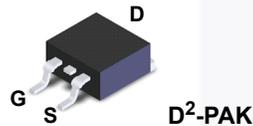
- Telecom/Server Power Supplies
- Solar Inverters
- Computing Power Supplies
- FPD TV Power/Lighting

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance.

SuperFET® II FRFET® MOSFET combines a faster and more rugged intrinsic body diode performance with fast switching, aimed at achieving better reliability and efficiency especially in resonant switching applications.

SuperFET® II FRFET® is very suitable for the switching power applications such as server/telecom power, Solar inverter, FPD TV power, computing power, lighting and industrial power applications.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCB110N65F	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	35
		- Continuous ( $T_C = 100^\circ\text{C}$ )	24
$I_{DM}$	Drain Current	- Pulsed (Note 1)	105
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	809
$I_{AR}$	Avalanche Current	(Note 1)	8
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	3.57
dv/dt	MOSFET dv/dt	(Note 3)	100
	Peak Diode Recovery dv/dt		50
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	357
		- Derate Above $25^\circ\text{C}$	2.86
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCB110N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> Pad of 2-oz copper), Max.	40	

FCB110N65F — N-Channel SuperFET® II FRFET® MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Tape Width
FCB110N65F	FCB110N65F	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	650	-	-	V
		$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}, T_J = 150^\circ\text{C}$	700	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.72	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	110	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.5\text{ mA}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 17.5\text{ A}$	-	96	110	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 17.5\text{ A}$	-	30	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3680	4895	pF
$C_{oss}$	Output Capacitance		-	110	145	pF
$C_{riss}$	Reverse Transfer Capacitance		-	0.65	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	65	-	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	464	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}$	-	98	145	nC
$Q_{gs}$	Gate to Source Gate Charge		-	20	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	43	-
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.7	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$	-	31	72	ns
$t_r$	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	89	188	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	5.7	21

### Drain-Source Diode Characteristics

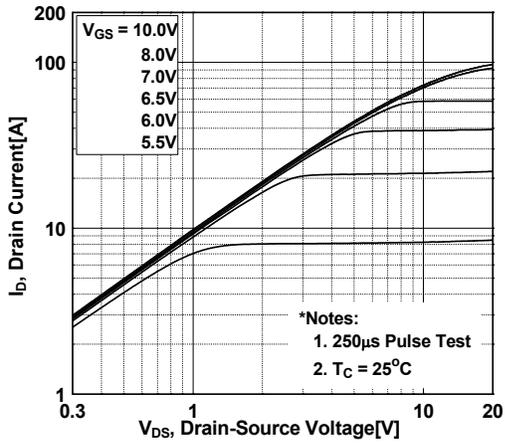
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	35	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	100	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 17.5\text{ A}$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 17.5\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	133	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	0.67	-	$\mu\text{C}$

#### Notes:

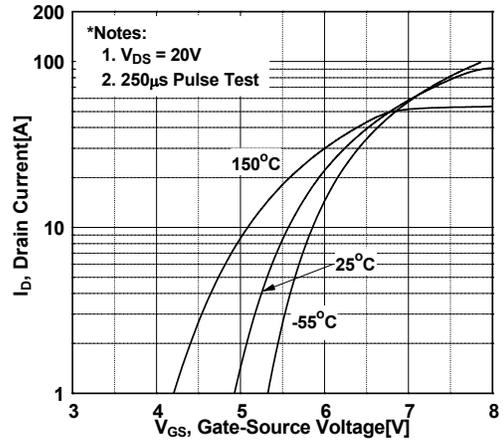
1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 8\text{ A}, R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 17.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

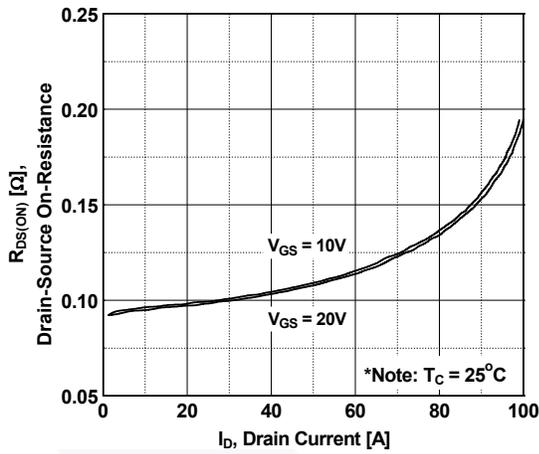
**Figure 1. On-Region Characteristics**



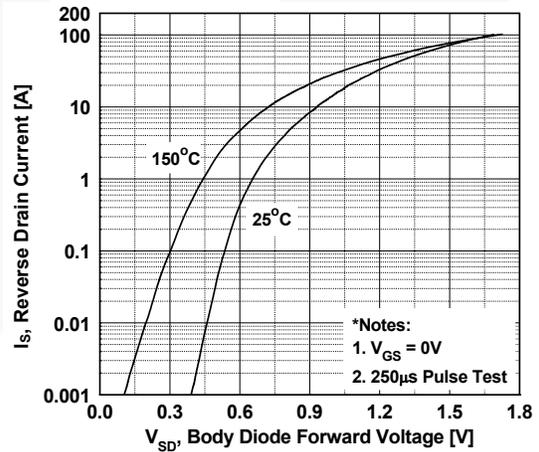
**Figure 2. Transfer Characteristics**



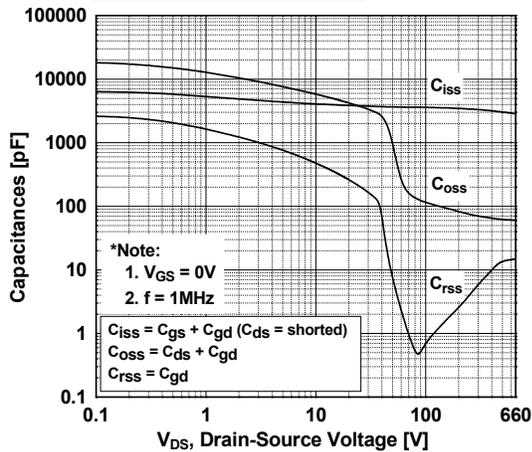
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



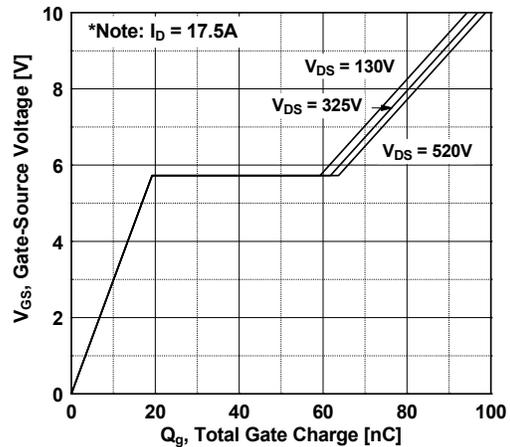
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

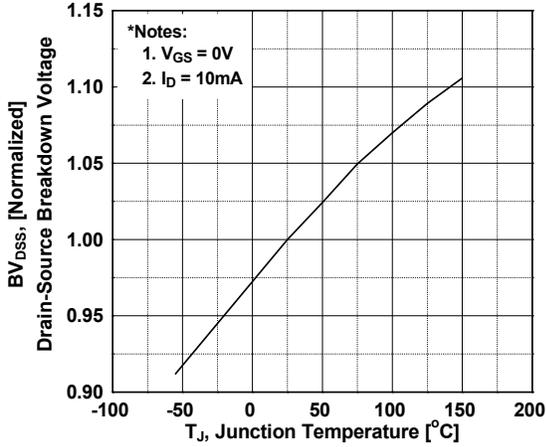


**Figure 6. Gate Charge Characteristics**

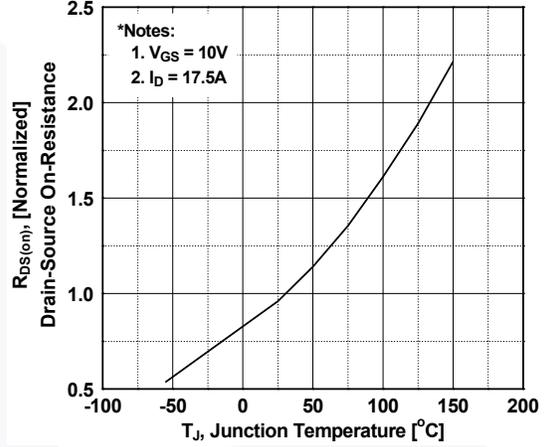


**Typical Performance Characteristics** (Continued)

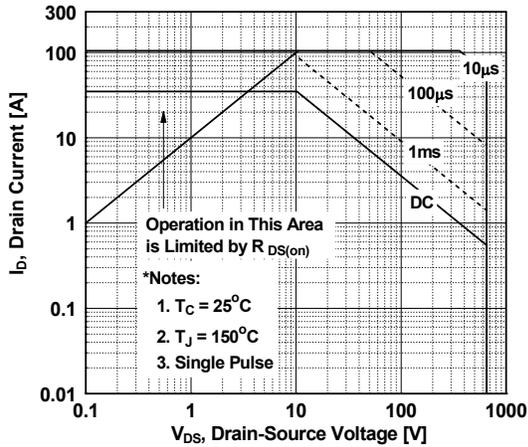
**Figure 7. Breakdown Voltage Variation vs. Temperature**



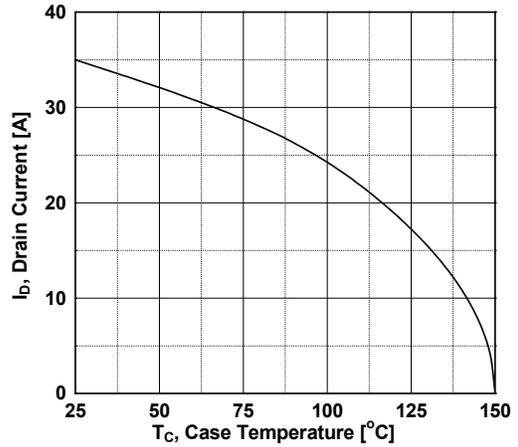
**Figure 8. On-Resistance Variation vs. Temperature**



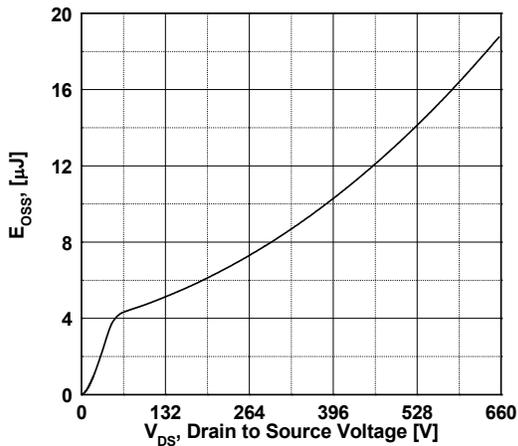
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

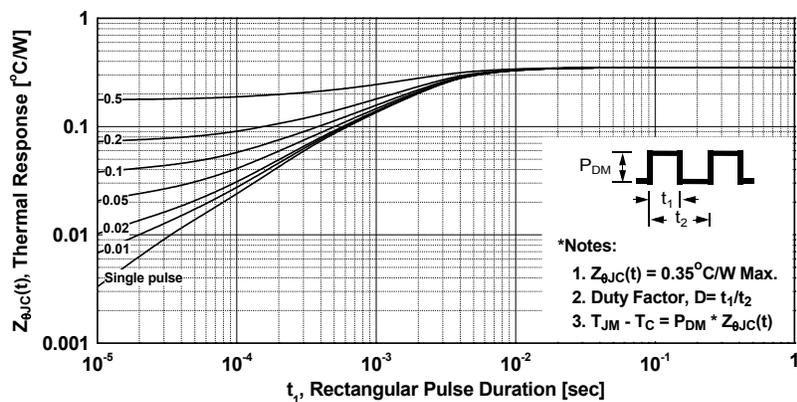


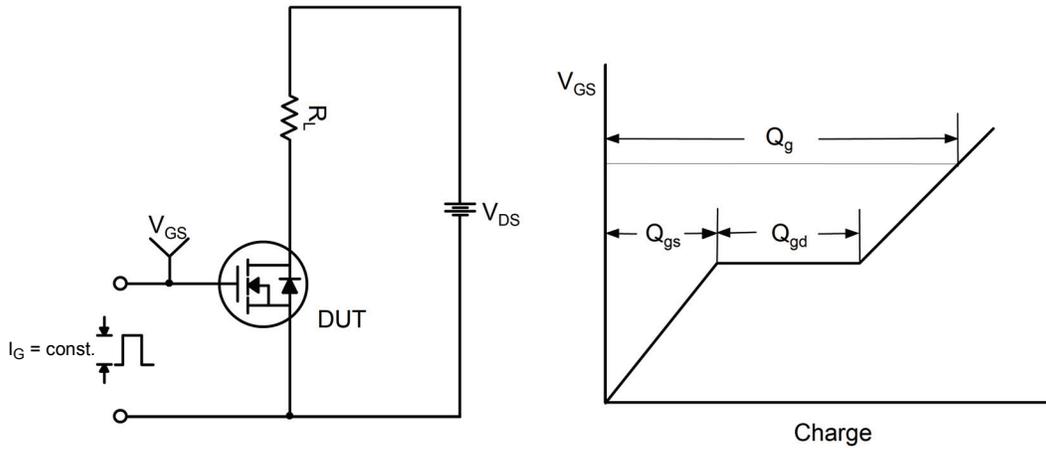
**Figure 11. E\_oss vs. Drain to Source Voltage Switching Capability**



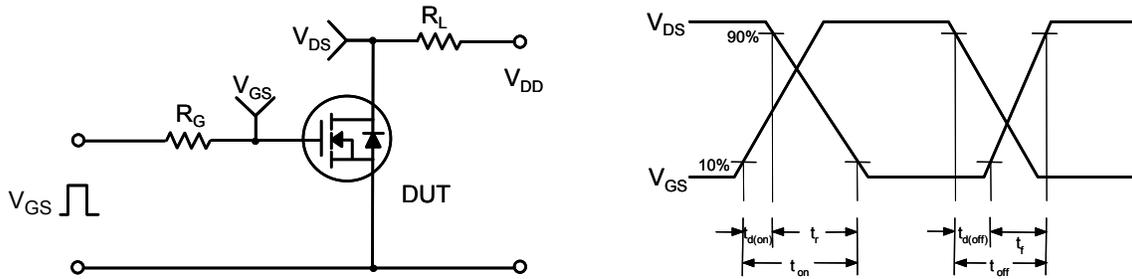
Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

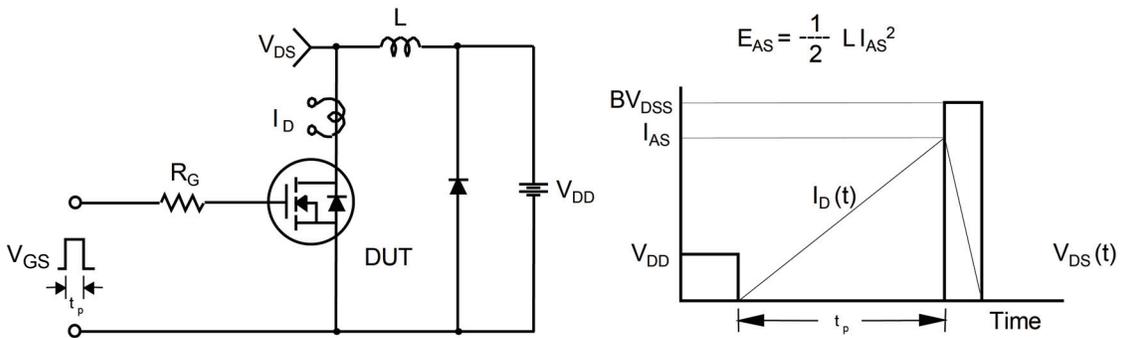




**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

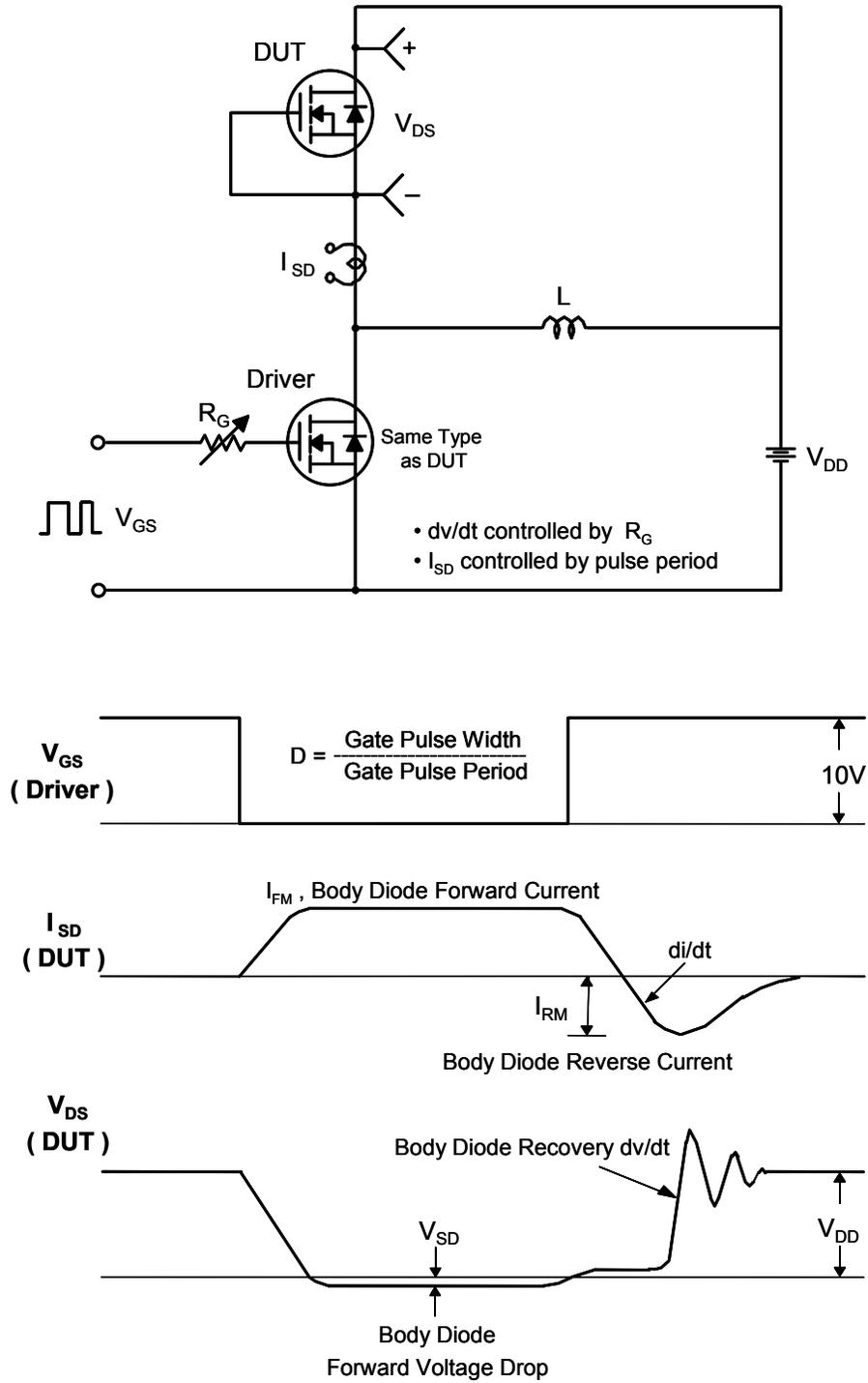
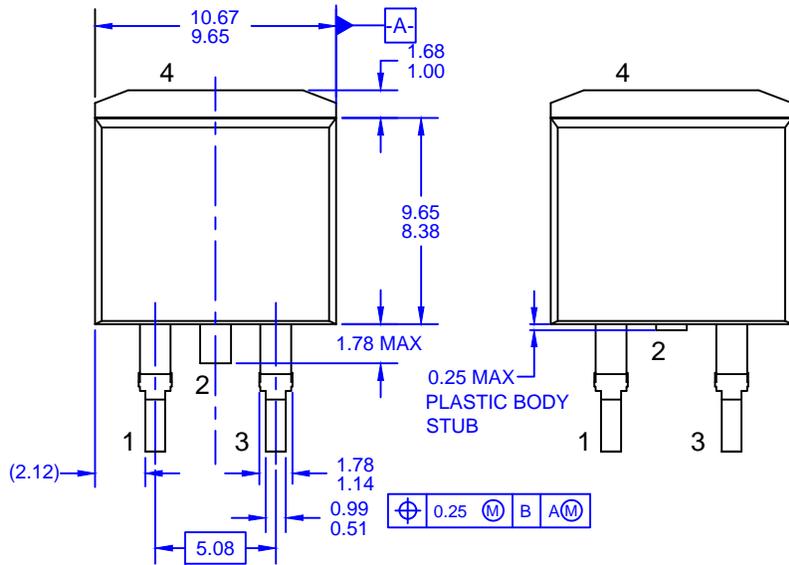
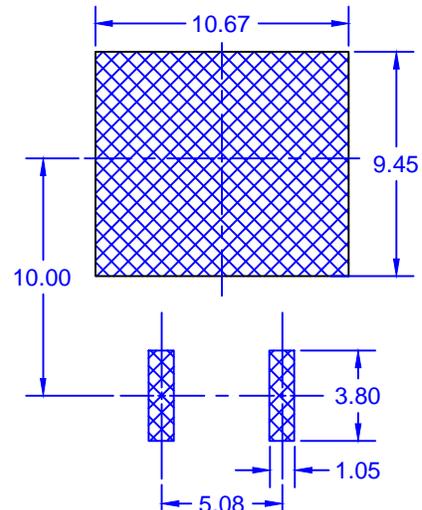


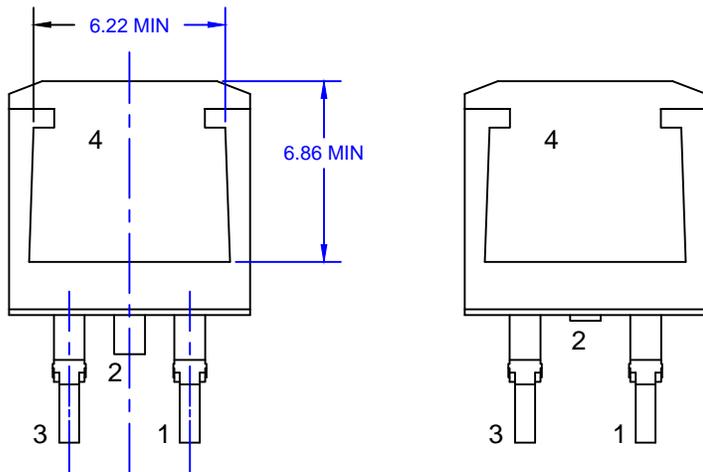
Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



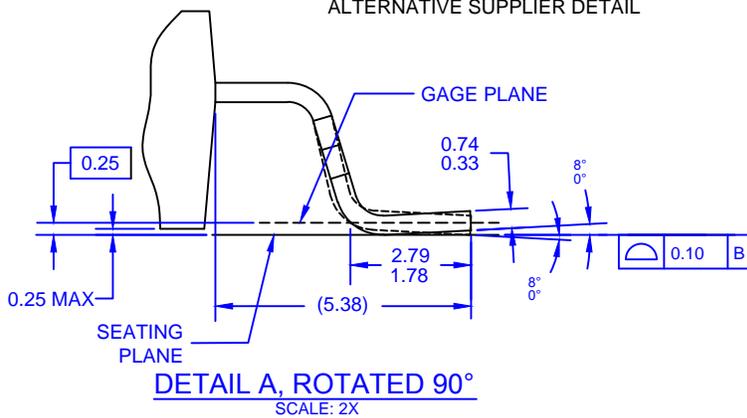
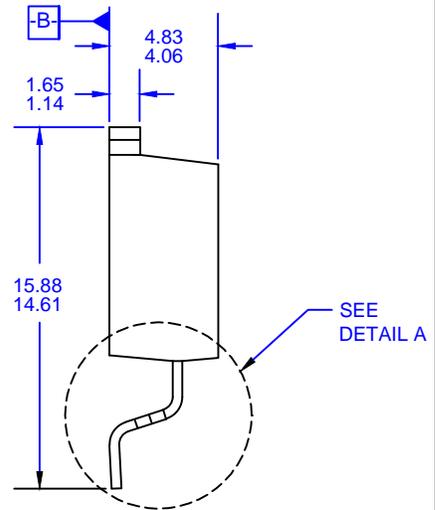
FRONT VIEW - DIODE PRODUCTS VERSION  
ALTERNATIVE SUPPLIER DETAIL



LAND PATTERN RECOMMENDATION  
UNLESS NOTED, ALL DIMS TYPICAL



BACK VIEW - DIODE PRODUCTS VERSION  
ALTERNATIVE SUPPLIER DETAIL



DETAIL A, ROTATED 90°  
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) REFERENCE JEDEC, TO-263, VARIATION AB.
- C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
- D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
- E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
- F) FILENAME: TO263A02REV8



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