MOSFET – Power, P-Channel, ChipFET

-20 V, -5.3 A

Features

- Low R_{DS(on)}
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package
- Pb-Free Package is Available

Applications

Power Management in Portable and Battery-Powered Products; i.e.,
 Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit
Drain-Source Voltage	V _{DS}	-2	20	V
Gate-Source Voltage	V _{GS}	±	12	V
Continuous Drain Current $(T_J = 150^{\circ}C)$ (Note 1) $T_A = 25^{\circ}C$ $T_A = 85^{\circ}C$	I _D	-5.3 -3.8	-3.9 -2.8	A
Pulsed Drain Current	I _{DM}	±	20	Α
Continuous Source Current (Note 1)	I _S	-5.3	-3.9	А
Maximum Power Dissipation (Note 1) T _A = 25°C T _A = 85°C	P _D	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	–55 to	+150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

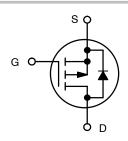
 Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



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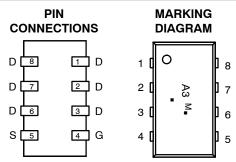
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX	
–20 V	46 mΩ @ -4.5 V	-5.3 A	



P-Channel MOSFET



ChipFET CASE 1206A STYLE 1



A3 = Specific Device Code

M = Month Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTHS5441T1	ChipFET	3000/Tape & Reel
NTHS5441T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit
Maximum Junction–to–Ambient (Note 2) t ≤ 5 sec Steady State	$R_{ hetaJA}$	40 80	50 95	°C/W
Maximum Junction-to-Foot (Drain) Steady State	$R_{ hetaJF}$	15	20	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Min Typ	Max	Unit
Static	-			-	•	
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-0.6		-1.2	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1.0	μΑ
		$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V},$ $T_{J} = 85^{\circ}\text{C}$			-5.0	
On-State Drain Current (Note 3)	I _{D(on)}	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = -4.5 \text{ V}$	-20			Α
Drain-Source On-State Resistance (Note 3)	r _{DS(on)}	$V_{GS} = -3.6 \text{ V}, I_D = -3.7 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -3.9 \text{ A}$	- -	0.050 0.046	0.06 -	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -3.1 \text{ A}$		0.070	0.083	
Forward Transconductance (Note 3)	9fs	$V_{DS} = -10 \text{ V}, I_{D} = -3.9 \text{ A}$		12		mhos
Diode Forward Voltage (Note 3)	V_{SD}	I _S = -2.1 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic (Note 4)						
Total Gate Charge	Q_{G}			9.7	22	nC
Gate-Source Charge	Q _{GS}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_{D} = -3.9 \text{ A}$		1.2		
Gate-Drain Charge	Q_{GD}			3.6		
Input Capacitance	C _{iss}			710		pF
Output Capacitance	C _{oss}	$V_{DS} = -5.0 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$ f = 1.0 MHz		400		
Reverse Transfer Capacitance	C _{rss}	<u>-</u>		140		
Turn-On Delay Time	t _{d(on)}			14	30	ns
Rise Time	t _r	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega$		22	55	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong -1.0 \text{ A}, V_{GEN} = -4.5 \text{ V},$ $R_G = 6 \Omega$		42	100	
Fall Time	t _f			35	70	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.1 A, di/dt = 100 A/μs		30	60	

Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).
 Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

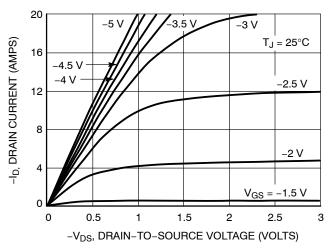


Figure 1. On-Region Characteristics

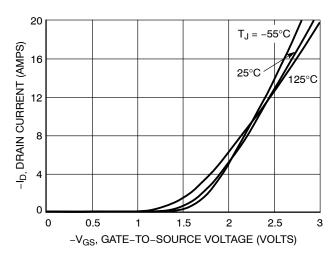


Figure 2. Transfer Characteristics

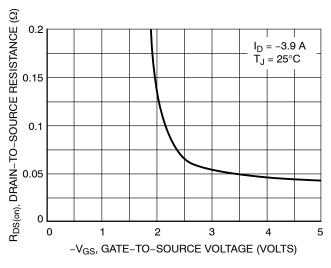


Figure 3. On–Resistance versus Gate–to–Source Voltage

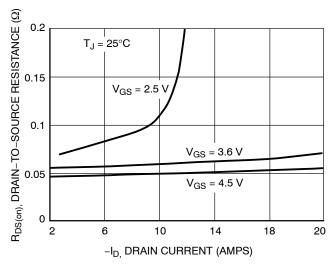


Figure 4. On-Resistance versus Drain Current and Gate Voltage

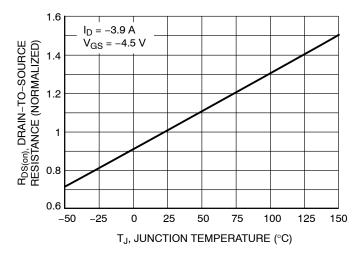


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

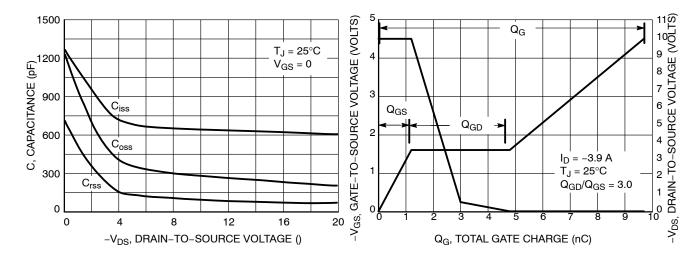


Figure 6. Capacitance Variation

Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

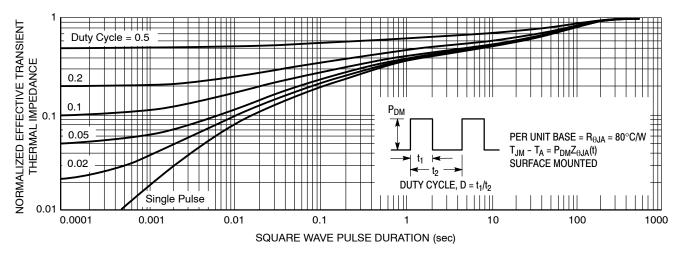


Figure 8. Normalized Thermal Transient Impedance, Junction-to-Ambient

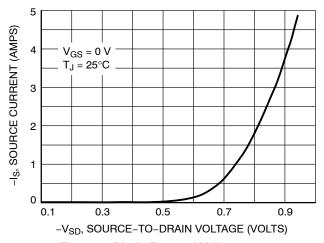
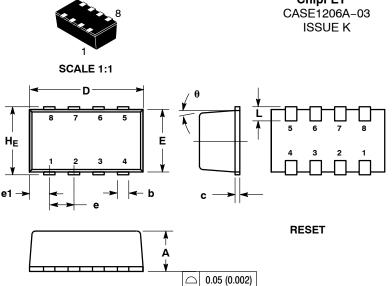


Figure 9. Diode Forward Voltage versus Current



ChipFET™

DATE 19 MAY 2009

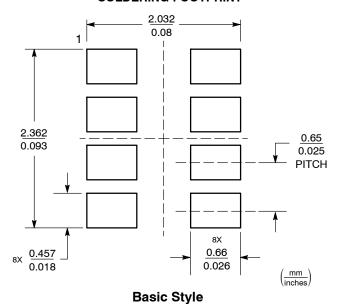
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL
- AND VERTICAL SHALL NOT EXCEED 0.08 MM.
 DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
- NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD
- SURFACE.

	MILLIMETERS				INCHES	
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
С	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
е		0.65 BSC			0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM				5° NOM	

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:	STYLE 6:
PIN 1. DRAIN	PIN 1. SOURCE 1	PIN 1. ANODE	PIN 1. COLLECTOR	PIN 1. ANODE	PIN 1. ANODE
DRAIN	GATE 1	2. ANODE	COLLECTOR	ANODE	2. DRAIN
DRAIN	SOURCE 2	SOURCE	COLLECTOR	DRAIN	3. DRAIN
GATE	4. GATE 2	4. GATE	4. BASE	DRAIN	4. GATE
SOURCE	5. DRAIN 2	5. DRAIN	EMITTER	SOURCE	SOURCE
DRAIN	6. DRAIN 2	6. DRAIN	COLLECTOR	6. GATE	6. DRAIN
7. DRAIN	7. DRAIN 1	CATHODE	COLLECTOR	CATHODE	7. DRAIN
8. DRAIN	8. DRAIN 1	CATHODE	COLLECTOR	CATHODE	8. CATHODE / DRAIN

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



= Specific Device Code XXX

М = Month Code

= Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

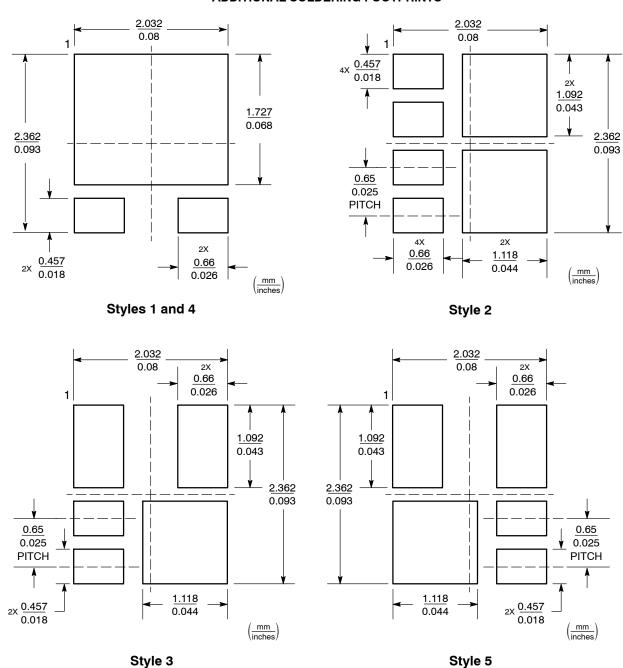
OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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DATE 19 MAY 2009

ADDITIONAL SOLDERING FOOTPRINTS*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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