SUNTSU

Real Time Clock Module

SRC32C Series

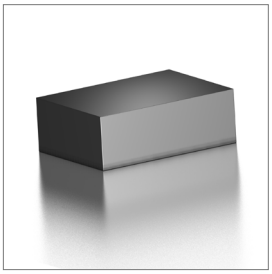
3.2mm x 2.5mm

Features

- Low Power Consumption
- High Stability
- I²C Interface
- Built in Temperature Sensor
- Backup Battery Switchover Function

Applications

- Smart Grid
- Ethernet
- Display
- Various Wireless Communicaiton



Part Numbering Guide

S RC 32 C N - 32.768K

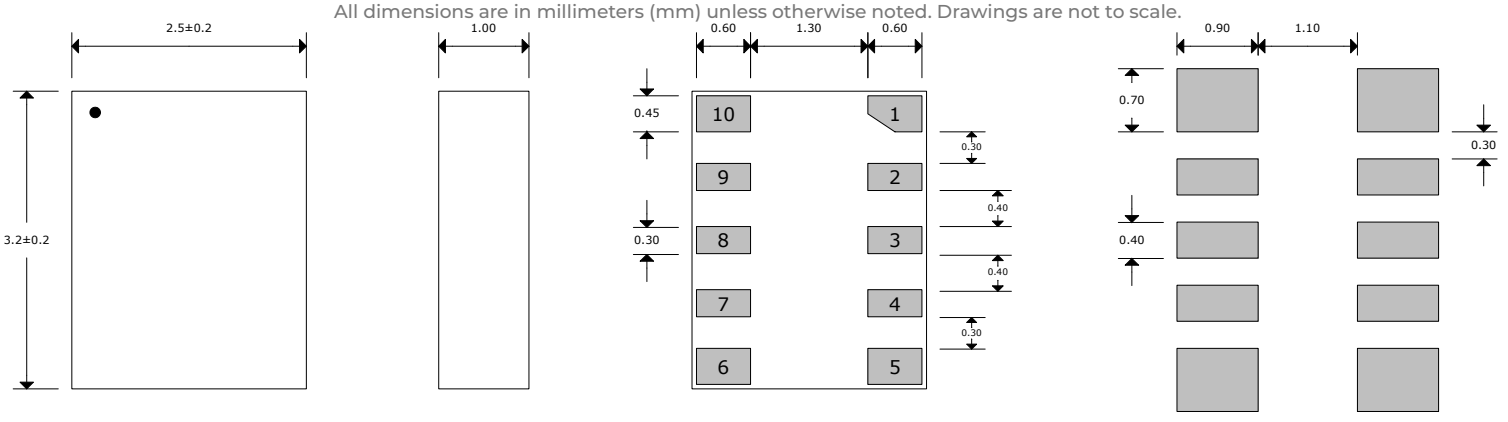
- SUNTSU
- REAL TIME CLOCK
- 3.2mm x 2.5mm
- OUTPUT: C : CMOS
- STABILITY: N : ±5.0ppm
- FREQUENCY: KHZ

RoHS COMPLIANT

Electrical Parameters	Units	Minimum	Typical	Maximum	Remarks
Frequency	KHz		32.768		
Frequency Stability vs. Op Temp	ppm	-5.0		5.0	-20°C ~ 70°C
	ppm	-20.0		20.0	-40°C ~ -20°C; 70°C ~ 85°C
Aging per Year	ppm			±3	
Operating Temperature	°C	-40		85	
Storage Temperature	°C	-55		125	
Supply Voltage (V_{DD})	V	2.5	3.0	5.0	Normal Operation
	V	1.6	3.0	5.0	In case of Single Supply
Current Consumption (I_{DD})	uA		2.0	3.0	
Symmetry (Duty Cycle)	%	1		99	32768Hz@50% V_{DD}
	%	45	50	55	1024Hz@50% V_{DD}
	%	45	50	55	1Hz@50% V_{DD}
Start Up Time	s			1	at 25°C
I/O Input Voltage (SCI, SDA Input)	V	GND-0.3		5.5	
I/O Input Voltage (FOE Input)	V	GND-0.3		5.5	
Clock Output Voltage (FOUT Output)	V	GND-0.3		V_{DD}+0.3	
I/O Output Voltage (SDA, /INT Output)	V	GND-0.3		5.5	
Temperature Sensor Accuracy	°C			±5	V_{DD}=3.0V

Outline Drawing

All dimensions are in millimeters (mm) unless otherwise noted. Drawings are not to scale.



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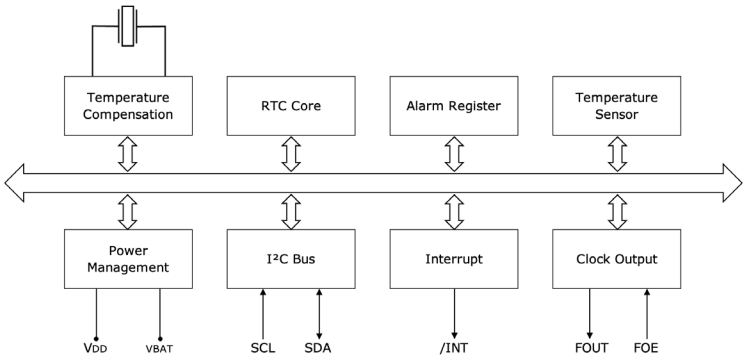
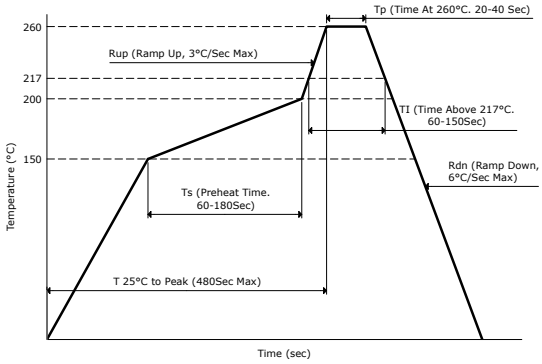
Block Diagram



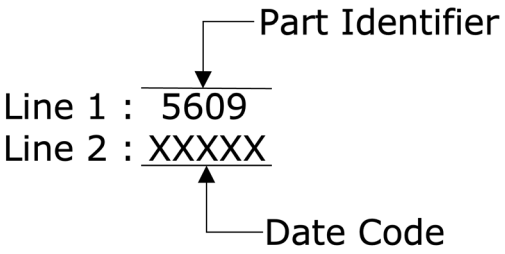
Pin Functions

PIN	FUNCTION	I/O	Description
1	FOE	In	FOUT output control pin. "1" -enable FOUT, "0"-FOUT Hi-Z
2	VDD	-	Power Supply
3	VBAT	-	battery. Connect to VDD when switchover function is not necessary
4	FOUT	Out	Frequency Output. Controlled by FOE. Frequency can be set by FSEL bits.
5	SCL	In	I²C clock signal
6	T1	-	Manufacture test only. Ensure to be floating
7	SDA	In/Out	I²C data signal
8	T2	-	Manufacture test only. Ensure to be floating
9	GND	-	Ground
10	/INT	Out	Interrupt Output, Open-Drain

Reflow Profile



Part Marking



Tape And Reel Dimensions

3,000pcs/Reel

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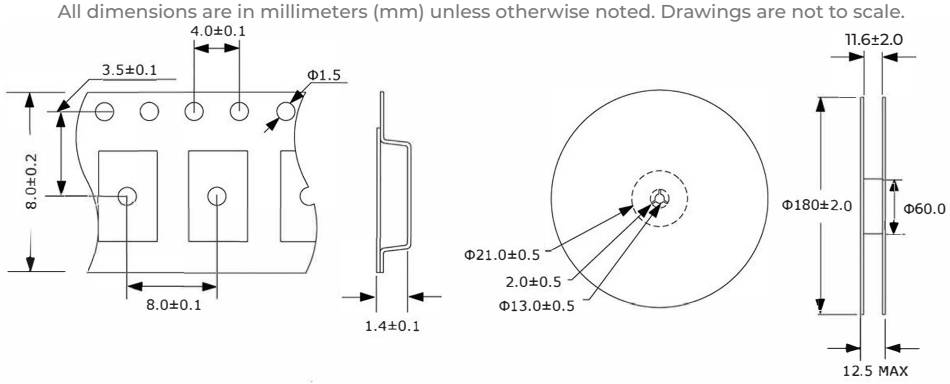

Environmental Specifications		Mechanical Specifications	
Temperature Cycling	MIL-STD-883, Method 1010, Condition B	Mechanical Shock	MIL-STD-202, Method 213, Condition B
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	Vibration	MIL-STD-883, Method 2007, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	Moisture Resistance	MIL-STD-883, Method 1004
Solderability	MIL-STD-883, Method 2003	Resistance to Solvents	MIL-STD-202, Method 215
Moisture Sensitivity	J-STD-020, MSL 1	Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K

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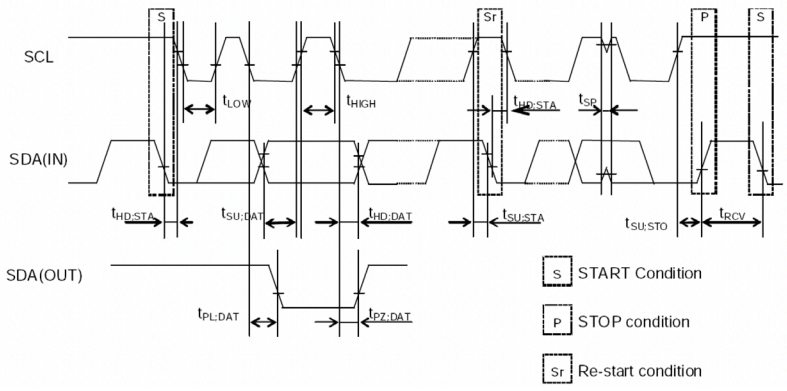
DC Characteristics	Units	Minimum	Typical	Maximum	Remarks
Average Current Consumption (V_{DD}=5V)	uA	0.91		5.1	fSCL=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation interval 2s
Average Current Consumption (V_{DD}=3V)	uA	0.88		4.9	fSCL=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation interval 2s
Average Current Consumption (V_{DD}=5V)	uA			20	fSCL=0Hz, FOE=VDD, /INT = VDD; VDD=VBAT; FOUT:32.768kHz, CL=0pF;
Average Current Consupption (V_{DD}=3V)	uA			19	Compensation interval 2s
Average Current Consumption (V_{DD}=5V)	uA	0.9		5.0	fSCL=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation off
Average Current Consumption (V_{DD}=3V)	uA	0.87		4.8	fSCL=0Hz, FOE=GND, /INT = VDD; VDD=VBAT; FOUT off (High-Z); Compensation off
High Level Input Voltage	V	0.8*V_{DD}		5.0	SCL, SDA, FOE Pin
Low Level Input Voltage	V	GND-0.3		0.2*V_{DD}	SCL, SDA, FOE Pin
High Level Output Voltage (FOUT Pin)	V	4.0		5.0	V_{DD}=5V, I_{OH}=-1mA
High Level Output Voltage (FOUT Pin)	V	2.2		3.0	V_{DD}=3V, I_{OH}=-1mA
High Level Output Voltage (FOUT Pin)	V	2.9		3.0	V_{DD}=3V, I_{OH}=-100uA
Low Level Output Voltage (FOUT Pin)	V	GND		GND+0.5	V_{DD}=5V, I_{OL}=1mA
Low Level Output Voltage (FOUT Pin)	V	GND		GND+0.8	V_{DD}=3V, I_{OL}=1mA
Low Level Output Voltage (FOUT Pin)	V	GND		GND+0.1	V_{DD}=3V, I_{OL}=100uA
Low Level Output Voltage (/INT Pin)	V	GND		GND+0.25	V_{DD}=5V, I_{OL}=1mA
Low Level Output Voltage (/INT Pin)	V	GND		GND+0.4	V_{DD}=3V, I_{OL}=1mA
Low Level Output Voltage (SDA Pin)	V	GND		GND+0.4	V_{DD}≥3V, I_{OL}=3mA
Input Leakage Current	uA	-0.5		0.5	FOE, SDA, SCL Pin, V_{IN} = V_{DD} or GND
Output Leakage Current	uA	-0.5		0.5	FOUT, SDA, /INTpin, V_{IN} = V_{DD} or GND

AC Characteristics	Units	Minimum	Typical	Maximum	Remarks
SCL Clock Frequency	kHz			400	
SCL Low Level Time	uS	1.3			
SCL High Level Time	uS	0.6			
Start Condition Setup Time	uS	0.6			
Start Condition Hold Time	uS	0.6			
Stop Condition Setup Time	uS	0.6			
Bus Idle Time Between Start and Stop	uS	1.3			
Data Setup Time	ns	100			
Data Hold Time	ns	0			
SCL, SDA Rising Time	us			0.4	
SCL, SDA Falling Time	us			0.4	

I²C Bus Timing Chart



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Basic Time and Calendar Registers

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00	SEC	O	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
01	MIN	O	BCD code, Minutes tens place, 0-5			BCD code, Minutes ones place, 0-9				R/W
02	HOUR	O	O	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
03	WEEK	O	6	5	4	3	2	1	0	R/W
04	DAY	O	O	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
05	MONTH	O	O	O	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
06	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
07	RAM	●	●	●	●	●	●	●	●	R/W
08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				R/W
09	HOUR Alarm	AE	●	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	R/W
0A	DAY Alarm	AE	●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
0B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
0C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
0D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
0E	Flag Register	O	O	UF	TF	AF	O	VLF	VDET	R/W
0F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	O	O	RESET	R/W

Extended Register Group 1

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
10	SEC	O	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				R/W
11	MIN	O	BCD code, Minutes tens place, 0-5			BCD code, Minutes ones place, 0-9				R/W
12	HOUR	O	O	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				R/W
13	WEEK	O	6	5	4	3	2	1	0	R/W
14	DAY	O	O	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				R/W
15	MONTH	O	O	O	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				R/W
16	YEAR	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				R/W
17	TEMP	128	64	32	16	8	4	2	1	R
18	Backup Function	O	O	O	O	VDET OFF	SWOFF	BKSMP [1]	BKSMP [0]	R/W
19	Not Use	O	O	O	O	O	O	O	O	R
1A	Not Use	O	O	O	O	O	O	O	O	R
1B	Timer Counter 0	128	64	32	16	8	4	2	1	R/W
1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	R/W
1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	R/W
1E	Flag Register	O	O	UF	TF	AF	O	VLF	VDET	R/W
1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	O	O	RESET	R/W

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Extended Register Group 2										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
20	Device ID	Vendor ID [3:0]				Ver [3:0]				R
21	RSV	Reserved: Ensure to be 0x80				O	O	O	VBATSW	R/W
22-26	RSV	Reserved: Ensure to be 0x00								R
27	SubSEC	Reserved				SubSEC [3:0]				R
28-30	RSV	Reserved: Ensure to be 0x00								R/W

Note: After the initial power-up or in case VLF bit returns "1", make sure to initialize all registers to default state before using the RTC. Ensure all inputs are in the required range and the defined values are set for the reserved bits in case the clock cannot work normally.

- During the initial power-up, below bits will be in the state as below:

  Initial 0:TEST, WADA, USEL, TE, FSEL[1:0], TSEL[0], UF, TF, AF, CSEL[1], UIE, TIE, RESET, VDETOFF, SWOFF, BKSMP[1:0], BKDET, VBATSW, VBDETEN, VBDETSEL[3:0].

  Initial 1: VLF, VDET, CSEL[0].

- All other register values are undefined, so make sure to reset the module before using it.
- The bits marked with "O" must be initialized to 0.
- The bits marked with "●" are RAM bits which can be used to write or read any data.
- Only 0 can be written to UF, TF, AF, VLF, VDET bits.
- Make sure "0" to be written for TEST bits which are used for testing only.
- Reserved bits must be set to the defined values accordingly.

Clock Counter Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
00/10	SEC	O	BCD code, Second tens place, 0-5			BCD code, Second ones place, 0-9				0x25
01/11	MIN	O	BCD code, Minutes tens place, 0-5			BCD code, Minutes ones place, 0-9				0x36
02/12	HOUR	O	O	BCD code, Hour tens place, 0-2		BCD code, Hour ones place, 0-9				0x01

SEC: BCD format, Value: 0~59
MIN: BCD format, Value: 0~59
HOUR: BCD format, Value: 0~23

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
03/13	WEEK	O	6	5	4	3	2	1	0	0x40

WEEK: Value 01h, 02h, 04h, 08h, 10h, 20h, 40h.
Only one bit can be set to 1 each time, all others must be set to 0.

WEEK Register									
WEEK	Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SUNDAY	01h	0	0	0	0	0	0	0	1
MONDAY	02h	0	0	0	0	0	0	1	0
TUESDAY	04h	0	0	0	0	0	1	0	0
WEDNESDAY	08h	0	0	0	0	1	0	0	0
THURSDAY	10h	0	0	0	1	0	0	0	0
FRIDAY	20h	0	0	1	0	0	0	0	0
SATURDAY	40h	0	1	0	0	0	0	0	0

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
04/14	DAY	O	O	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x01

DAY: BCD format, the value range can be adjusted automatically according to the size of the month and if it is a leap year or not.

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DAY Register Value	
Month	**Day Value Range**
1, 3, 5, 7, 8, 10, 12	1 ~ 31
4, 6, 9, 11	1 ~ 30
February in normal year	1 ~ 28
February in leap year	1 ~ 29

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
05/15	MONTH	O	O	O	BCD code, Month tens place, 0-1	BCD code, Month ones place, 0-9				0x01
03/13	WEEK	BCD code, Year tens place, 0-9				BCD code, Year ones place, 0-9				0x00

MONTH: BCD format, Value 1~12
YEAR: BCD format, Value 0~99 (2000~2099)

Example: January 01, 2021; 21:18:36

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00/10	SEC	O	0	1	1	0	1	1	0
01/11	MIN	O	0	0	1	1	0	0	0
02/12	HOUR	O	O	1	0	0	0	0	1
03/13	WEEK	O	0	0	0	1	0	0	0
04/14	DAY	O	O	0	0	0	0	0	1
05/15	MONTH	O	O	O	0	0	0	0	1
06/16	YEAR	0	0	1	0	0	0	0	0

Alarm Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
08	MIN Alarm	AE	BCD code, Minute tens place, 0-5			BCD code, Minute ones place, 0-9				0x00
09	HOUR Alarm	AE	●	BCD code, Minutes tens place, 0-5		BCD code, Minute ones place, 0-9				0x00
0A	WEEK Alarm	AE	6	5	4	3	2	1	0	0x00
0A	DAY Alarm	AE	●	BCD code, Day tens place, 0-3		BCD code, Day ones place, 0-9				0x00

According to AIE, AF, WADA bits setting, the alarm interrupt will be generated once the current time match the settings in the above registers, the /INT pin goes to low level and AF bit is set to '1' to record an alarm interrupt event has occurred.

AE: Alarm Enable bit, 0-enable; 1-disable
WADA bit controls the register 0x0A is Week alarm or Day alarm. The details can be found in 0x0D register bit6.
AF: Defined in 0x0E register bit3
AIE: Defined in 0x0F register bit3

Timer Control Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0B/1B	Timer Counter 0	128	64	32	16	8	4	2	1	0x00
0C/1C	Timer Counter 1	●	●	●	●	2048	1024	512	256	0x00

Cooperate with TE, TF, TIE, TSEL[1:0], a timer interrupt will be generated once the value countdown to 0 from the one set in the above registers.
TE: Defined in 0x0D register bit4
TF: Defined in 0x0E register bit4
TIE: Defined in 0x0F register bit4
TSEL[1:0]: Defined in 0x0D register bit1 and bit0

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Extension Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0D/1D	Extension Register	TEST	WADA	USEL	TE	FSEL [1]	FSEL [0]	TSEL [1]	TSEL [0]	0x02

To specify the alarm function or time update interrupt and FOUT output frequency etc.
TEST: test bit, can be set as “0” only.
WADA: Week Alarm/Day Alarm control bit, 1-DAY alarm, 0-WEEK alarm
USEL: Update Interrupt Select bit, output interrupt setting, 0-output interrupt once a second(default), 1-output interrupt once a Minute.
TE: Timer Enable bit, 1-enable timer interrupt function, 0-disable timer interrupt function.

FSEL [1]. FSEL [0]: FOUT frequency setting

FSEL [1]	FSEL [0]	FOUT Frequency
0	0	32.768KHz (Default)
0	1	1024Hz
1	0	1Hz
1	1	32.768KHz

TSEL [1], TSEL [0]: Timer countdown period (source clock) setting:

TSEL [1]	TSEL [0]	Source Clock
0	0	4096Hz
0	1	64Hz
1	0	1Hz
1	1	1/60Hz

Flag Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0E/1E	Flag Register	O	O	UF	TF	AF	O	VLF	VDET	0x23

UF: Update flag bit. It will be set to “1” when time update interrupt event occurs and keeps “1” until a “0” is written to it.
TF: Timer Flag bit. It will be set to “1” when a fixed-cycle timer interrupt event occurs and keeps “1” until a “0” is written to it.
AF: Alarm Flag bit. It will be set to “1” when an alarm interrupt event occurs and keeps “1” until a “0” is written to it.
VLF: Voltage Low Flag bit. When voltage is lower than 1.6V, this bit will be set to “1” and keeps “1” until a “0” is written to it.
VDET: Voltage Detection Flag bit. When voltage is lower than 1.95V, this bit will be set to “1” and keeps “1” until a “0” is written to it.

Control Registers										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0F/1F	Control Register	CSEL [1]	CSEL [0]	UIE	TIE	AIE	O	O	RESET	0x40

Control Register 1										
Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x21	Control Register 1	Reserved: Must be 0x8				O	O	O	VBATSW	0x80

CSEL [1]. CSEL [0]: Compensation interval Select 0, 1 bits, used to set temperature compensation interval

CSEL [1]	CSEL [0]	Compensation Interval
0	0	0.5s
0	1	2s (Default)
1	0	10s
1	1	30s

UIE: Update Interrupt Enable bit. When UF changs from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).
TIE: Timer Interrupt Enable bit: When TF changs from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).
AIE: Alarm Interrupt Enable bit: When AF changs from “0” to “1”, this bit controls if an interrupt signal is generated. 0-disable (/INT keeps Hi-Z), 1-enable(/INT status changes from Hi-Z to Low).
RESET: Reset IC, prepared for the synchronized starting of time or timer.

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Temperature Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
17	TEMP	128	64	32	16	8	4	2	1	0xa9

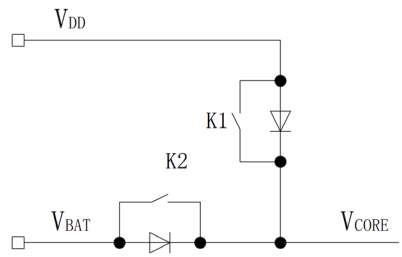
Read digital temperature data, Temp[°C] = (TEMP[7:0] * 2 -187.19) / 3.218.

Battery Backup Switchover Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
0x18	Backup Function	O	O	O	O	VDET OFF	SWOFF	BKSMP [1]	BKSMP [0]	0x00

This register controls the power switchover function.
Once abnormal V_{DD} is detected, it will be switched to use battery as the power supply.

Power Circuit Diagram



Battery Backup Switchover Register

V_{DD} Detect Function	VDETOFF	SWOFF	BKSMP [1]	BKSMP [0]	V_{DD} Voltage Sampling Time	Switch ON/OFF	Notes
On	0	X	0	0	2ms	2ms Off	Default
On	0	X	0	1	16ms	16ms Off	
On	0	X	1	0	128ms	128ms Off	
On	0	X	1	1	256ms	256ms Off	
Off	1	0	x	x	Off	On	K1 Close
Off	1	1	x	x	Off	Off	K1 Open

VDETOFF (Voltage Detector OFF): Main power supply V_{DD} voltage detection control bit. 0-enable detection function (Default), V_{DD} voltage will be detected once a second; 1-disenable detection function.
SWOFF (Switch OFF): Switch K1 control bit. 0- close (Default); 1- open BKSMP[1], BKSMP[0](Backup mode Sampling time): Control the voltage detection sampling time. Default: 00.

Device ID Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
20	Device ID	VendorID[3:0]				Ver[3:0]				0xd1

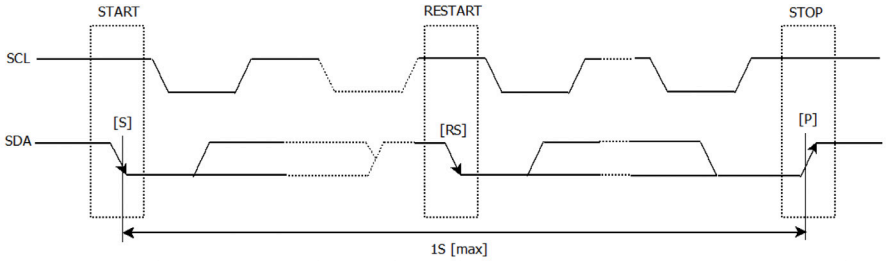
VendorID[3:0]: SRC32C's ID code, the fixed value is defined as VendorID[3:0]=1101b=Dh.
Ver[3:0]: version of the IC

Sub-second Timer Register

Address	Function	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Default
27	subSEC	Reserved				subSEC[3:0]				0x00

SubSEC[3:0]: sub second bit, and unit is 1/16s.

I²C Bus Interface



I²C bus supports bi-directional communications through a serial clock line SCL and a serial data line SDA. I²C bus device can be defined as "Master" and "Slave".
SRC32C can only be used as Slave.

I²C bus includes START, RESTART, STOP conditions, the duration between START and STOP must be less than 1 second just in case the bus to be set to standby mode automatically.
A new START condition must be transferred before restarting of any communications.

SRC32C I²C bus interface supports single byte read/write operations as well as multiple bytes incremental access.
After Ox7F address, the next one will be 0x00.

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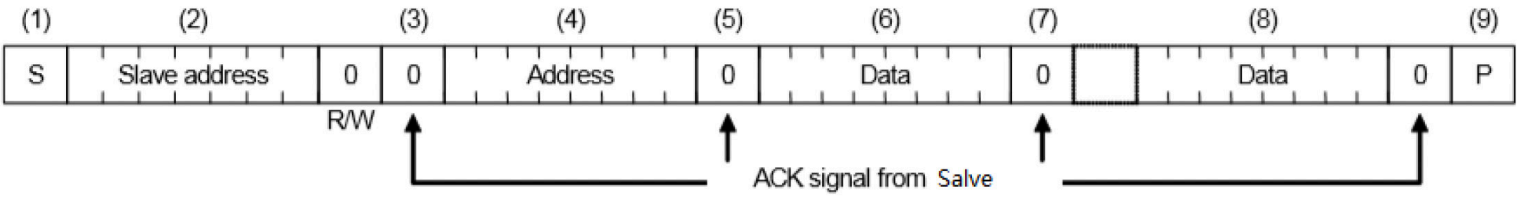
Slave Address									
Transfer Data	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
65h (Read)	0	1	1	0	0	1	0	1	Read
64h (Write)	0	1	1	0	0	1	0	0	Write

SRC32C I²C bus Slave Address is [0110 010*].

It is assumed CPU is master and SRC32C is slave in this section.

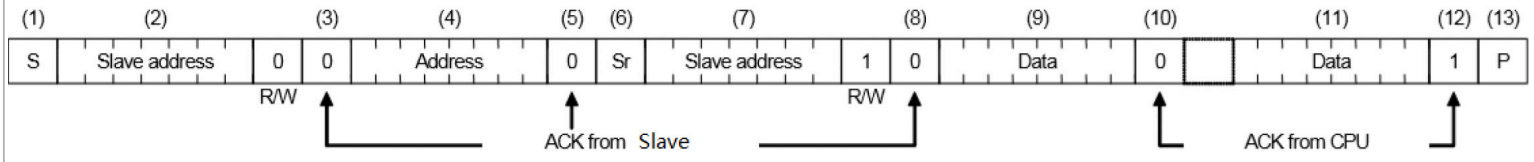
Write Process



I²C bus includes an address auto-increment function, once the initial address has been specified, the SRC32C increments (+1) the address automatically after each data is sent, then to write next data.

(1) CPU sends start condition[S]
(2) CPU sends SRC32C's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from SRC32C
(4) CPU sends write address to SRC32C
(5) CPU verifies ACK signal from SRC32C
(6) CPU sends write data to the address specified at step (4)
(7) CPU verifies ACK signal from SRC32C
(8) Repeat (6) (7) if multiple bytes need to be writen, address will be incremented automatically
(9) CPU ends stop condition[P]

Read Process



Writing the address to be read with write mode firstly, then reading the data with read mode.

(1) CPU sends start condition[S]
(2) CPU sends SRC32C's slave address with R/W bit to set to write mode
(3) CPU verifies ACK signal from SRC32C
(4) CPU sends address for reading from SRC32C
(5) CPU verifies ACK signal from SRC32C
(6) CPU sends RESTART condition [Sr]
(7) CPU sends SRC32C's slave address with R/W bit to set to read mode
(8) CPU verifies ACK signal from SRC32C
(9) CPU reads data from the specified address in step (4)
(10) CPU verifies ACK signal from SRC32C
(11) Repeat (9) (10) if multiple bytes need to be read, address will be incremented automatically
(12) CPU sends ACK signal for "1"
(13) CPU sends stop condition[P]

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